6.5810: Virtualization + Dune

Adam Belay <abelay@mit.edu>

Logistics

- Sign up for paper presentations
  - Due date has been updated to Sunday (9/18) to give more time
- If you haven’t already, create a CloudLab account

Plan for today

1. Dune:

- Exposes privileged CPU features, normally used to build kernels, safely to userspace

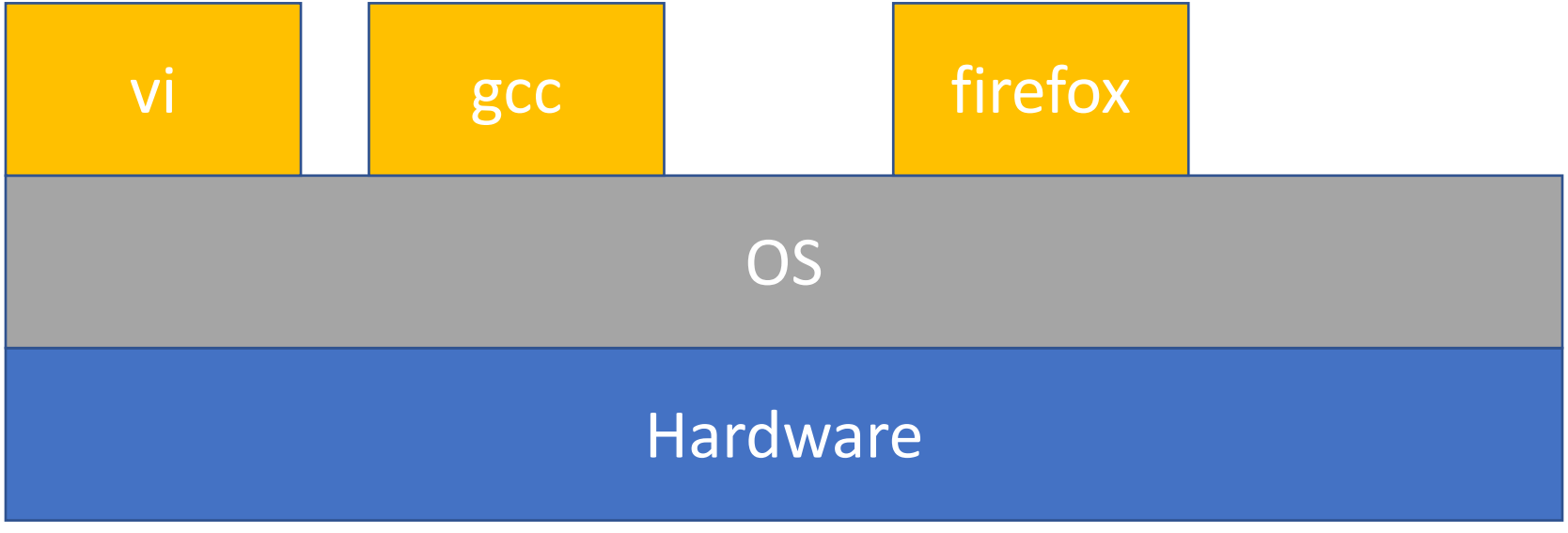
2. IO Virtualization:

- Allows programs to communicate with I/O hardware (e.g., networking and storage) directly and safely (not violating memory isolation)

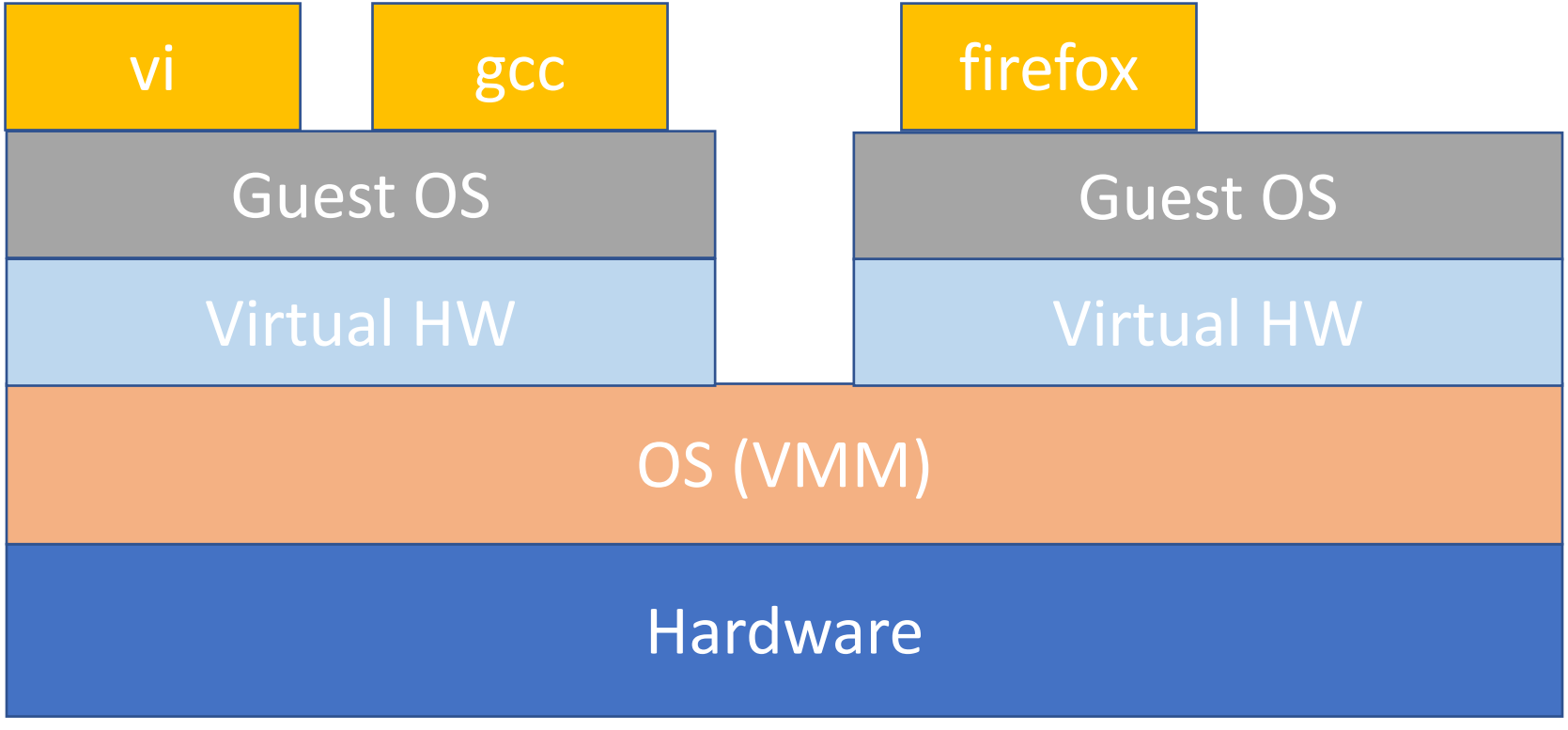
3. AIFM:

- Application-integrated far memory

Recap: Process Architecture



Recap: VM Architecture



- What if the process abstraction looked just like HW?

Comparing a process and HW

Process

- Non privileged registers and instructions
- Virtual memory
- Signals
- File system and sockets

Hardware

- All registers and instructions
- Virt. mem. and MMU
- Traps and interrupts
- I/O devices and DMA

Can a CPU be virtualized?

Requirements to be “virtualizable” defined by Popek and Goldberg in 1974:

1. **Fidelity**: Software on the VMM executes identically to its execution on hardware, barring timing effects.
2. **Performance**: An overwhelming majority of guest instructions are executed by the hardware without the intervention of the VMM.
3. **Safety**: The VMM manages all hardware resources.

Memory virtualization

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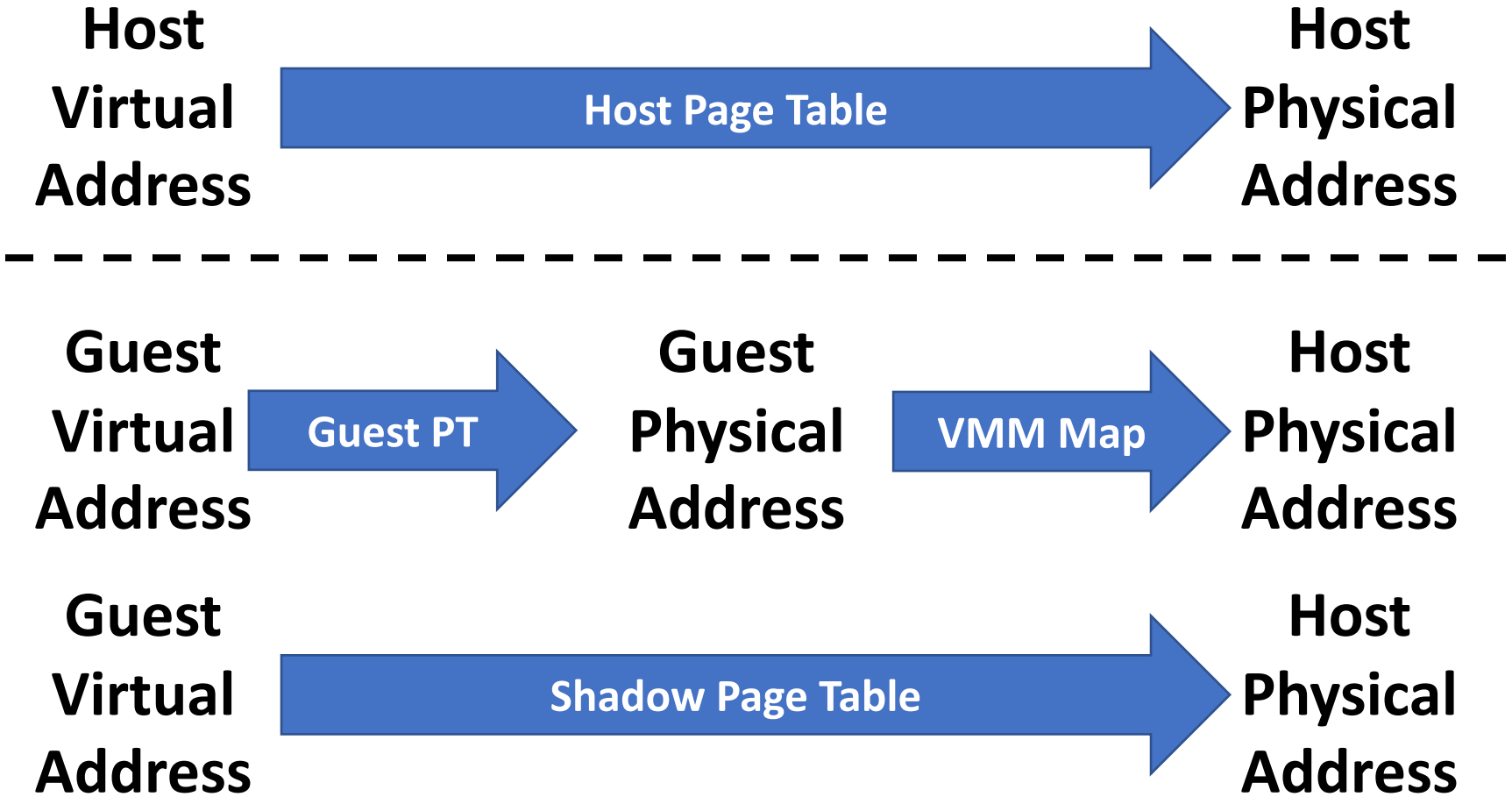


Why can’t the VMM let the VM guest kernel program the page table directly?

Trap-and-emulate is not possible on x86

Two problems:

1. Some instructions behave differently in user mode instead of trapping
2. Some registers leak state that reveals if the CPU is running in usermode

- Violates ***fidelity*** property
- Risc-V doesn’t have this problem!

Two possible solutions

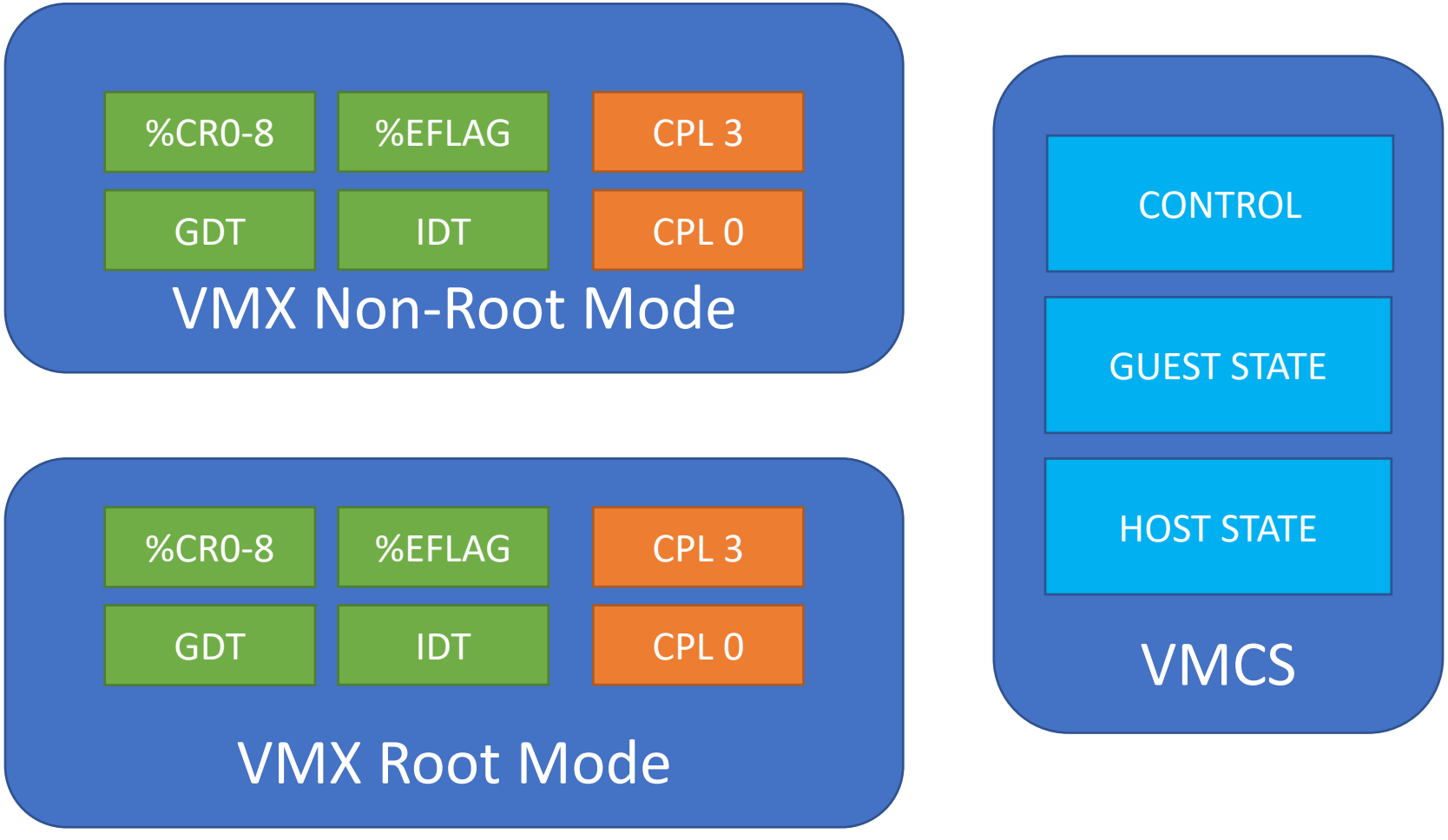
1. Binary translation
   - Rewrite offending instructions to behave correctly

2. Hardware virtualization
   - CPU maintains shadow state internally and directly executes privileged guest instructions

Intel VT-x

- Makes x86 hardware “virtualizable” under Popek and Goldberg definition
- Goal: **Direct execution** of most privileged instructions
- Introduces two CPU modes, kind of like ring protection
  - VMX Root Mode: For running VMM (host)
  - VMX Non-root Mode: For running VMs (guest)
  - But each mode has its own rings (user/kernel)
- In-memory structure called VMCS stores privileged register state and control flags

Intel VT-x


%CR0-8
%EFLAG
CPL 3
GDT
IDT
CPL 0
VMX Non-Root Mode
%CR0-8
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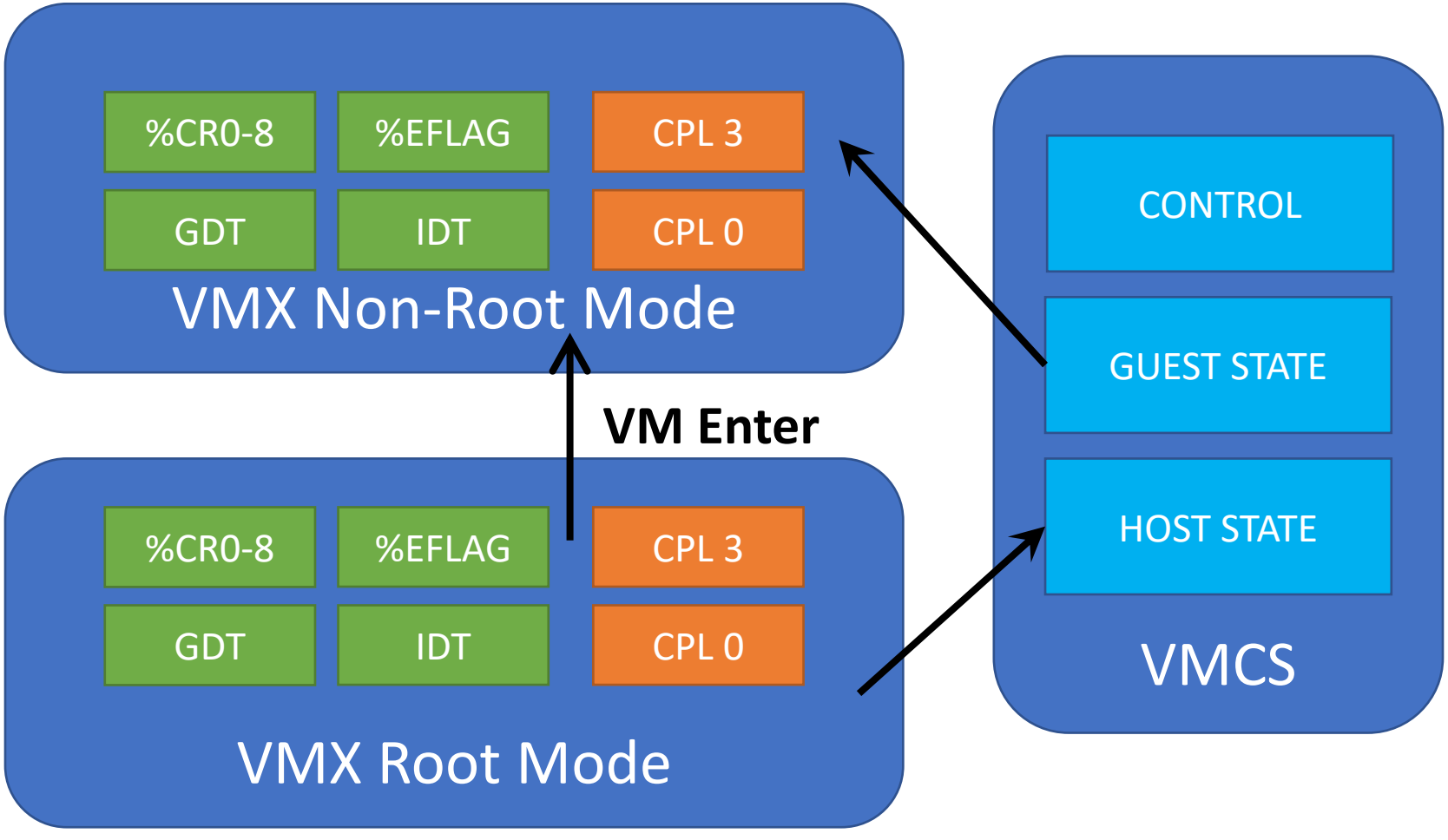
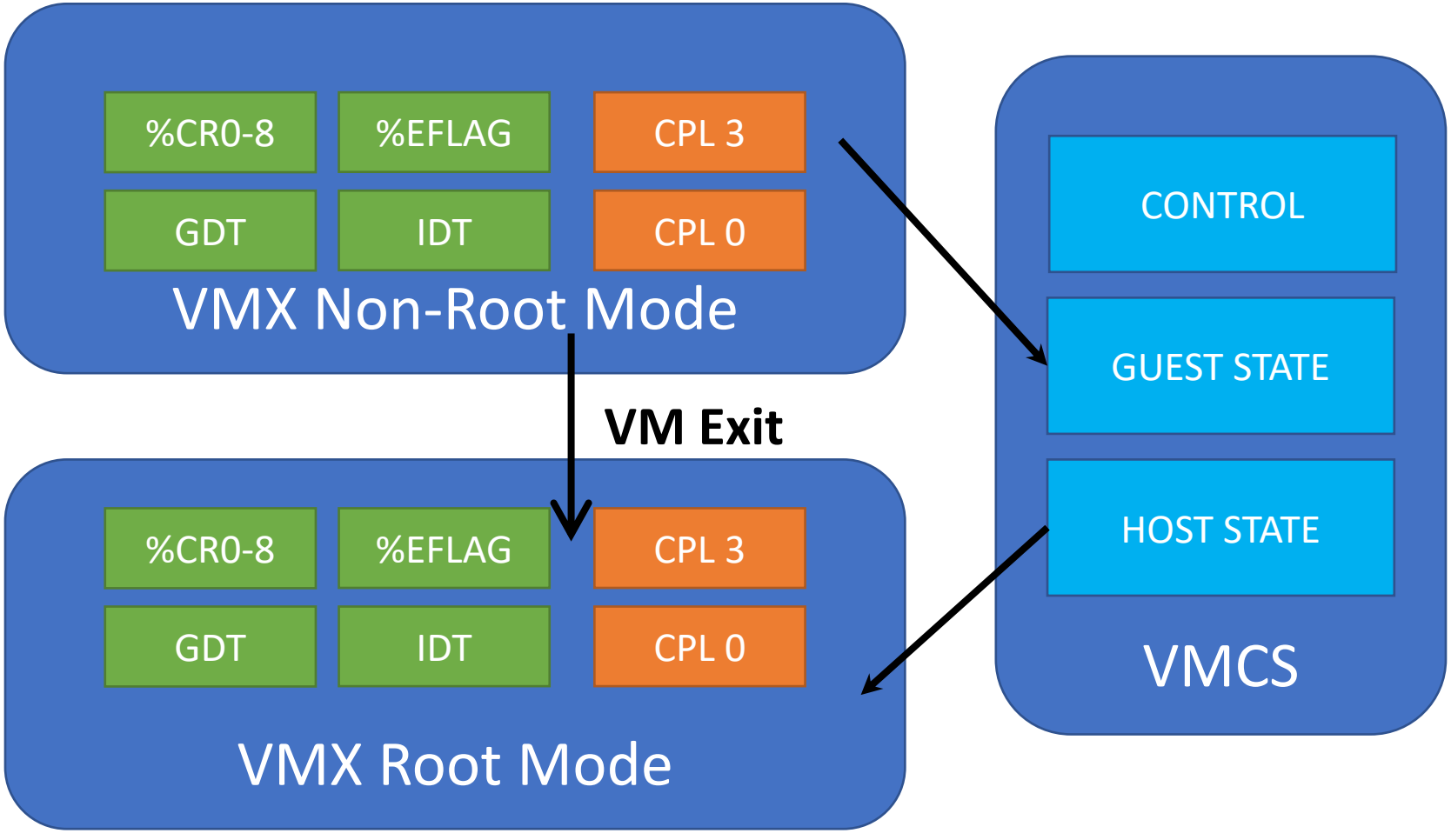
GDT
IDT
CPL 0
VMX Root Mode
CONTROL
GUEST STATE
HOST STATE
VMCS

Intel VT-x: VM Enter



Intel VT-x: VM Exit

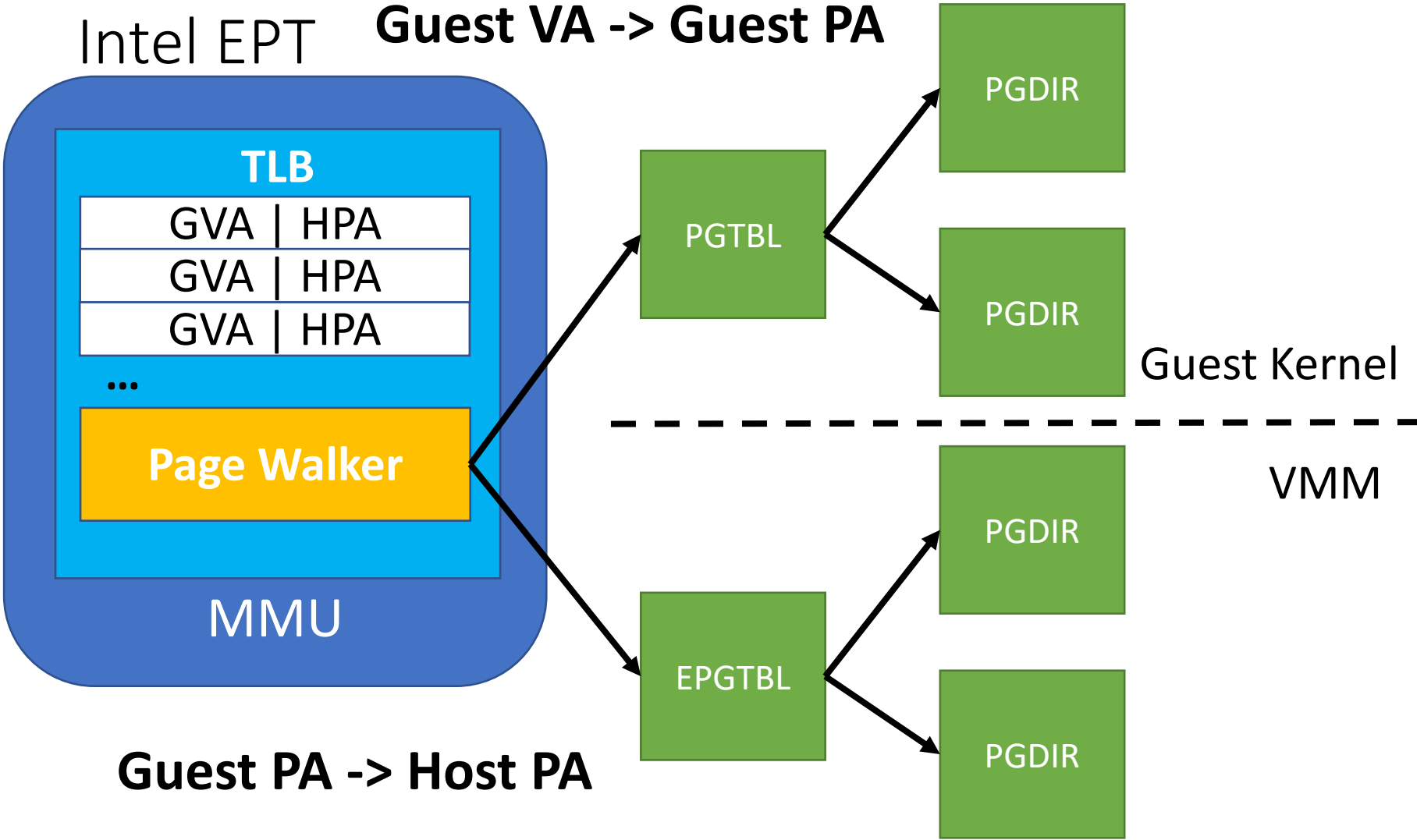


VM Enter and VM Exit

- Transitions between VMX Root Mode and VMX Non-root Mode
- VM Exit
  - VMCALL instruction, EPT Page Faults, some trap and emulate (configured in VMCS)
- VM Enter
  - VMLAUNCH instruction: Enter VMX Non-root Mode for a new VMCS
  - VMRESUME instruction: Enter VMX Non-root Mode for the last VMCS (faster)
- Typical VM Exit/Enter is ~200 cycles on modern HW

Intel EPT (nested paging)

- Goal: **Direct execution** of guest page table interactions
  - Reads and write to page table in memory
  - mov %eax, %cr3, INVLPG, etc.
- Idea: Maintain two layers of paging translation
  - Normal page table: Guest-virtual to guest-physical
  - EPT: guest-physical to host-physical

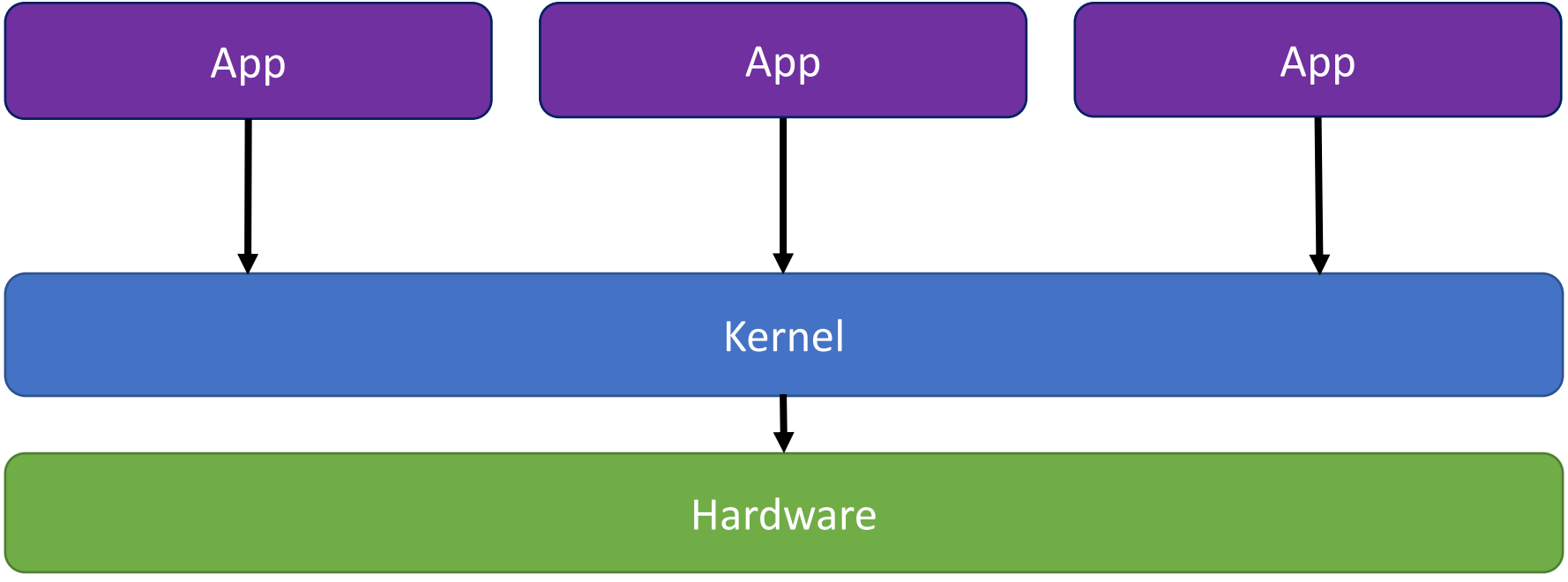

Intel EPT
Guest VA -> Guest PA
TLB
GVA | HPA
GVA | HPA
GVA | HPA
...
Page Walker
MMU
PGTBL
PGDIR
PGDIR
Guest Kernel
VMM
EPGTBL
PGDIR
PGDIR
Guest PA -> Host PA

Q: What’s faster EPT or Shadow Page Tables?

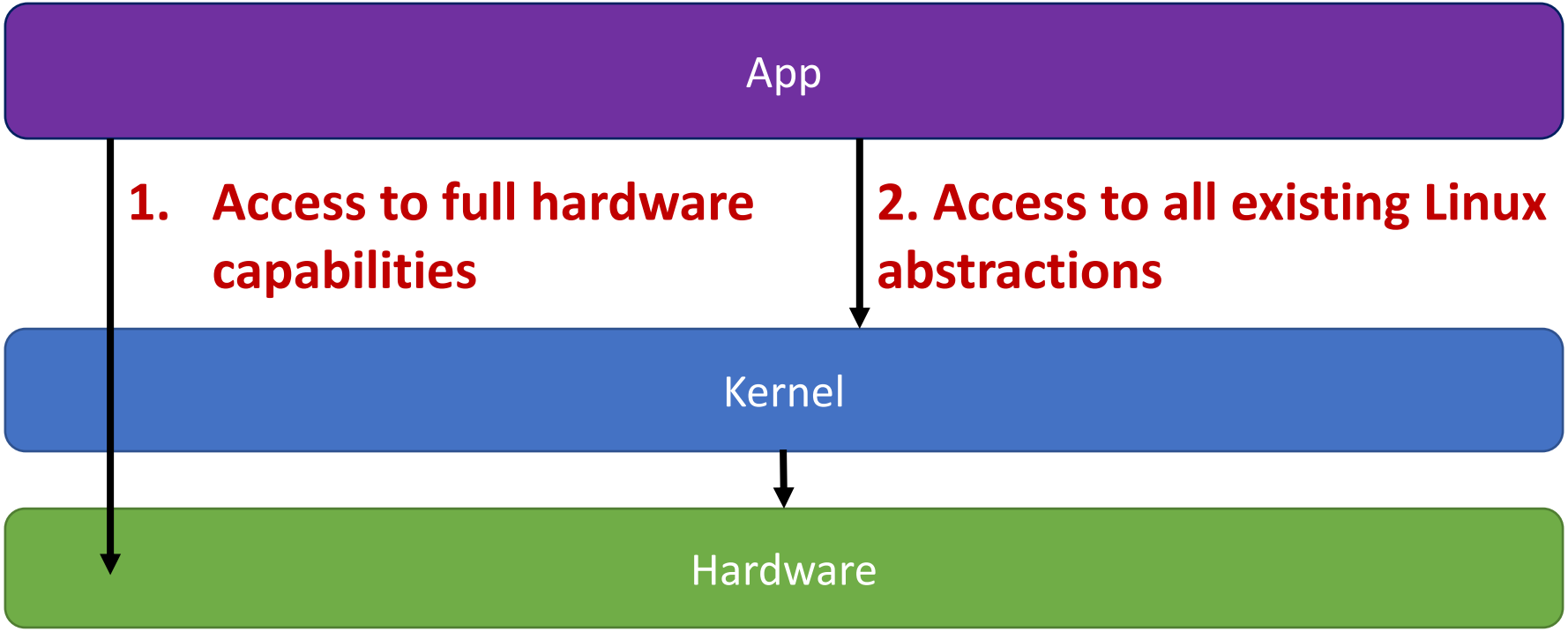
Big picture

- Direct execution reduces overhead
  - Avoids VM exits, trap-and-emulate, binary translation
- Enabled by microarchitectural changes:
  - Intel VT-x: direct execution of most privileged instructions (e.g. IDT, GDT, ring protection, EFLAG, etc.)
  - Intel EPT: direct execution of page table manipulation

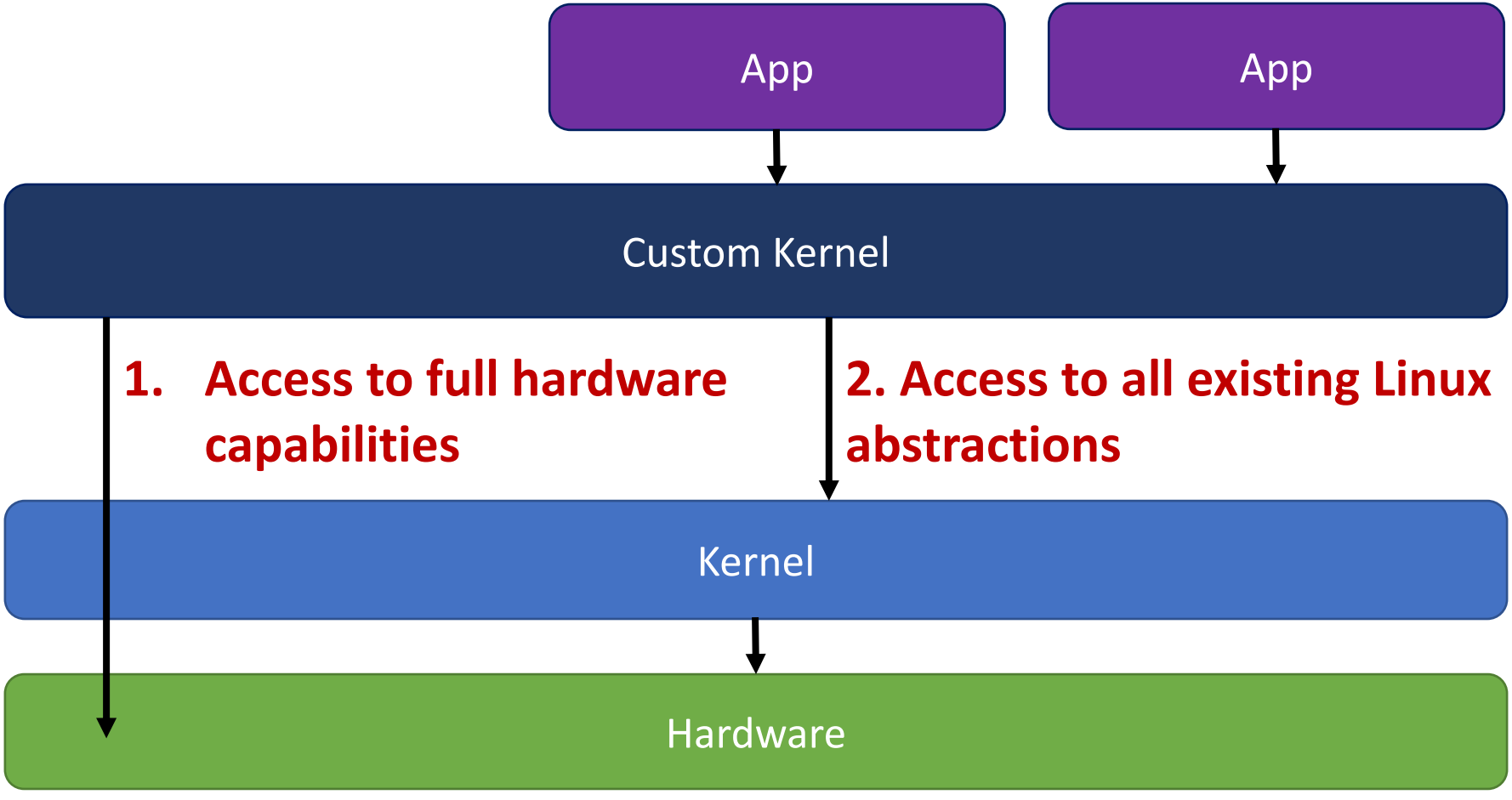
Operating systems today



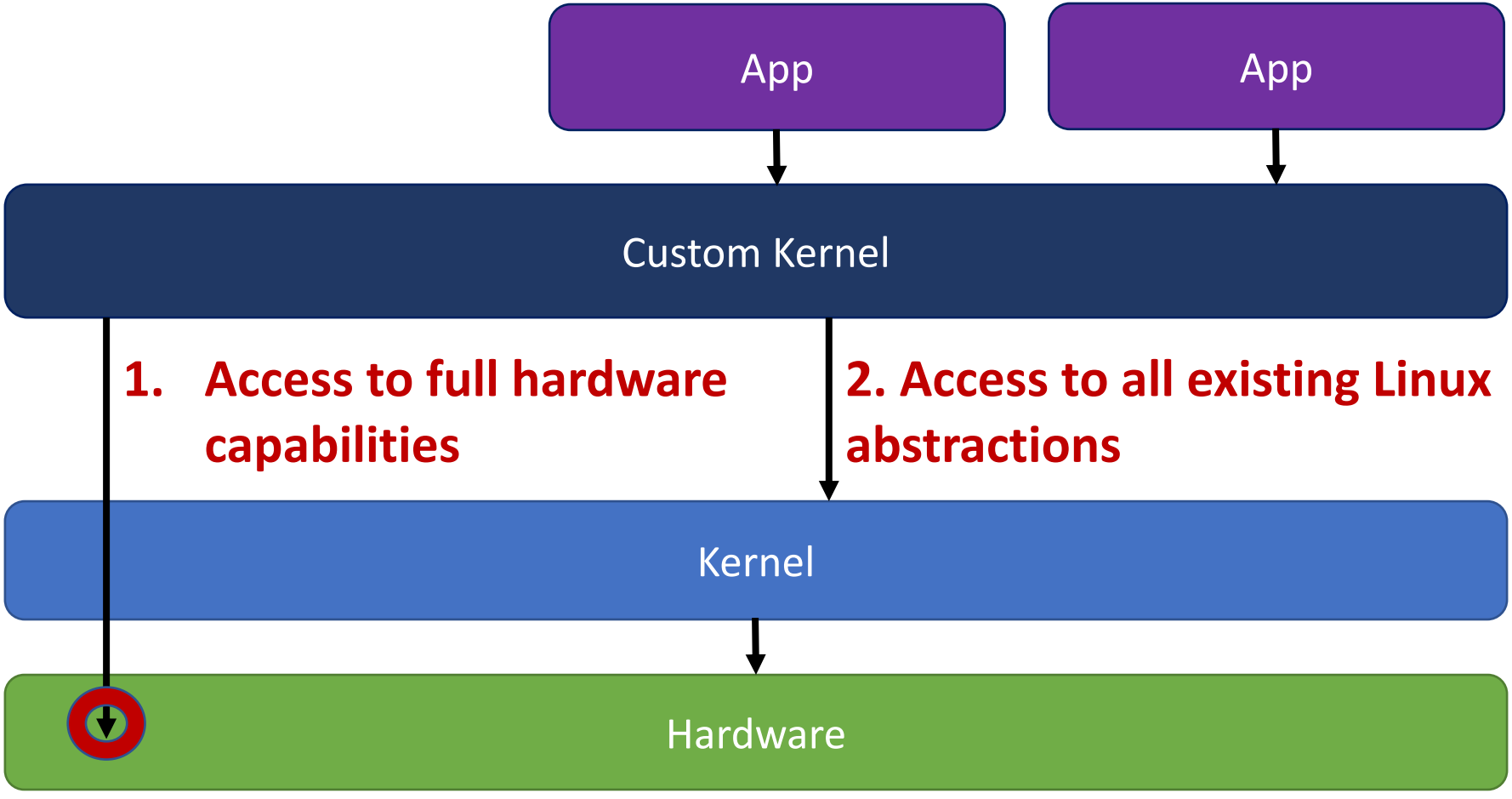
What if you could give a process access to raw hardware?



Could build new OS on top of Linux



But still must maintain process isolation



Dune

- Key Idea: Use VT-x, EPT, etc. to support Linux processes instead of virtual machines
- Dune is loadable kernel module, makes it possible for an ordinary Linux process to switch to “Dune mode”
- Dune mode processes can run along side ordinary processes.

A dune process

- Is still a process
  - has memory, can make Linux system calls, is fully isolated, etc.
- But isolated with VT-x Non-root mode
  - Rather than with CPL=3 and page table protections
- memory protection via EPT
  - Dune configures EPT so process can only access the same physical pages it would normally have access to

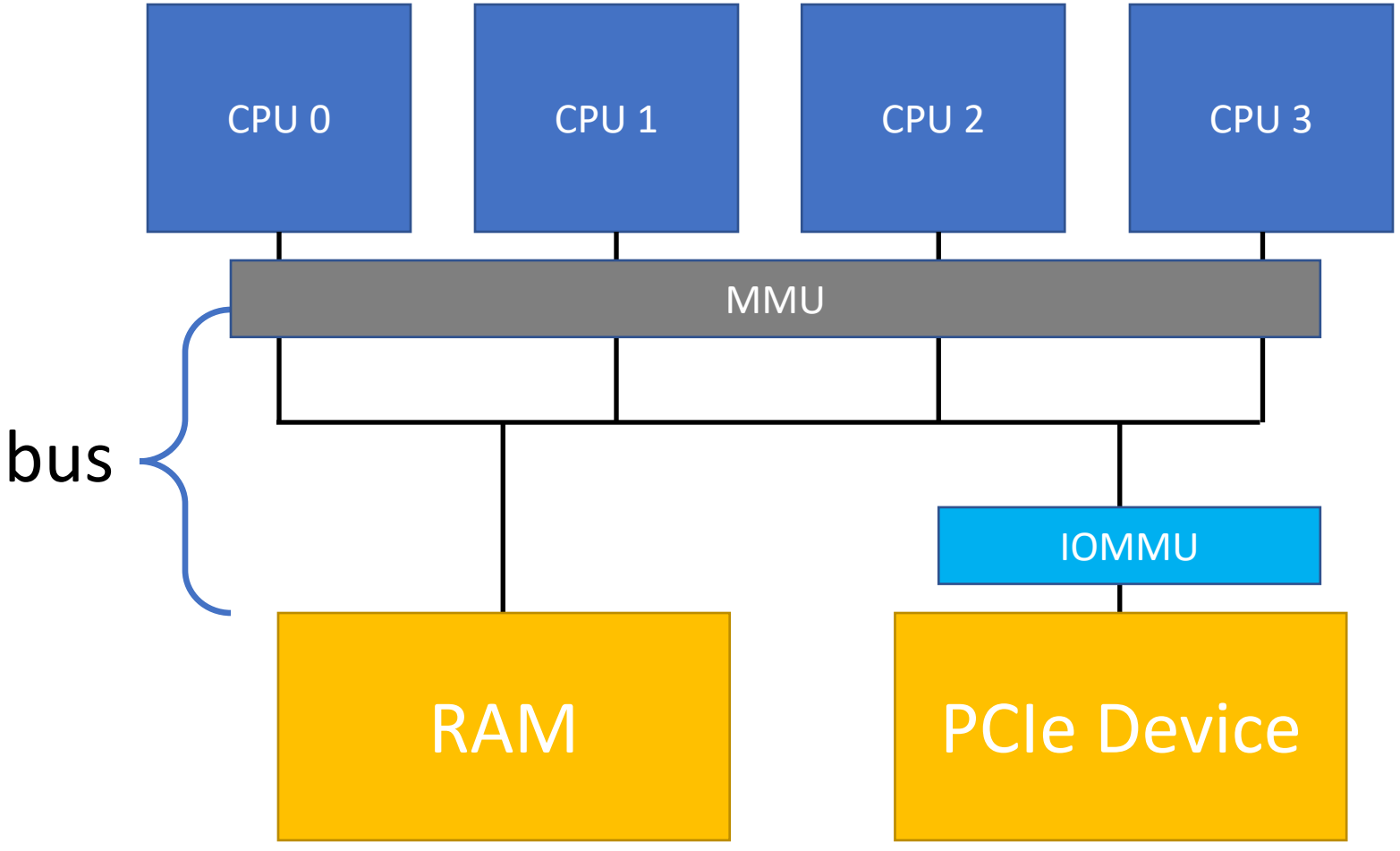
Why isolate a process with VT-x?

- Process can access all of Linux environment while also directly executing most privileged instructions
- User code now runs at CPL 0
- Process can manage its own page table via %CR3
- Fast exceptions (e.g. page faults) via shadow IDT
  - Kernel crossings eliminated
- Can run sandboxed code at CPL 3
  - So process can act like a kernel!

SR-IOV + IOMMU

- Goal: Allows **direction execution** of I/O device access
- Challenge #1: How to partition a single device into multiple instances
- Challenge #2: How to prevent DMA from overwriting memory belonging to VMM or another guest

IOMMU



Major challenges in practice

1. Memory: Traditionally must be pinned (cannot be swapped)
   - Pinning and unpinning is very expensive
2. Completions: Must be busy-polled (wastes CPU) or interrupt driven (high overhead)
   - Caladan offers a solution to this problem (next week)
3. Scalability: SR-IOV is HW intensive, IOTLB is limited in size
   - Today's IO devices degrade in performance beyond a certain scale

Conclusion

- VT-x and EPT enable direct execution of guest instructions
- Dune implements processes with VT-x and EPT rather than ordinary ring protection

AIFM: High-Performance, Application-Integrated Far Memory

Zain (Zhenyuan) Ruan[*] Malte Schwarzkopf [†] Marcos K. Aguilera [‡] Adam Belay[*]

[*]MIT CSAIL [†]Brown University [‡]VMware Research

In-Memory Applications

Data Analytics

Web Caching

Database

Graph Processing

Memory Is Inelastic

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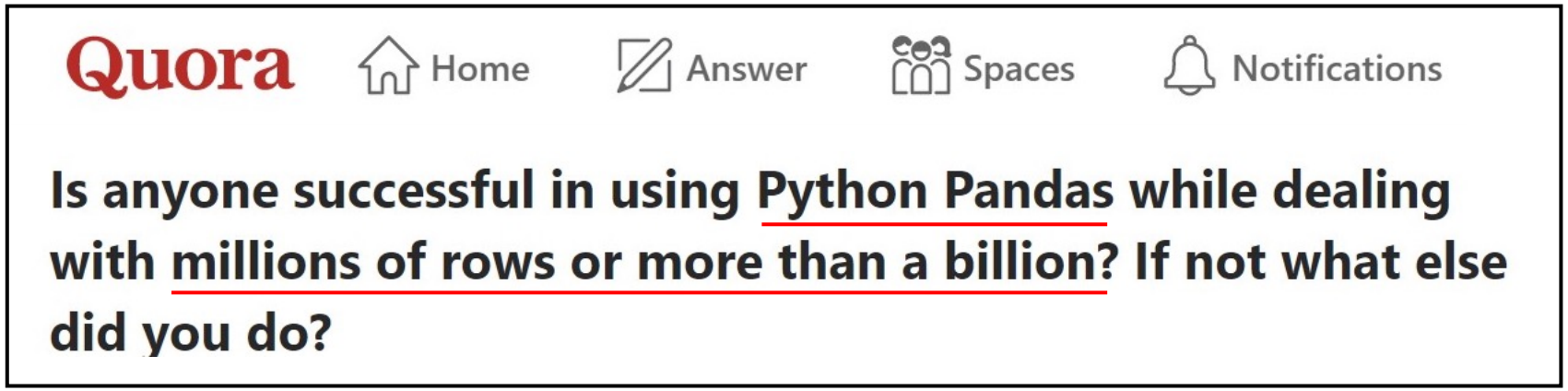
➢Applications cannot overcommit memory.



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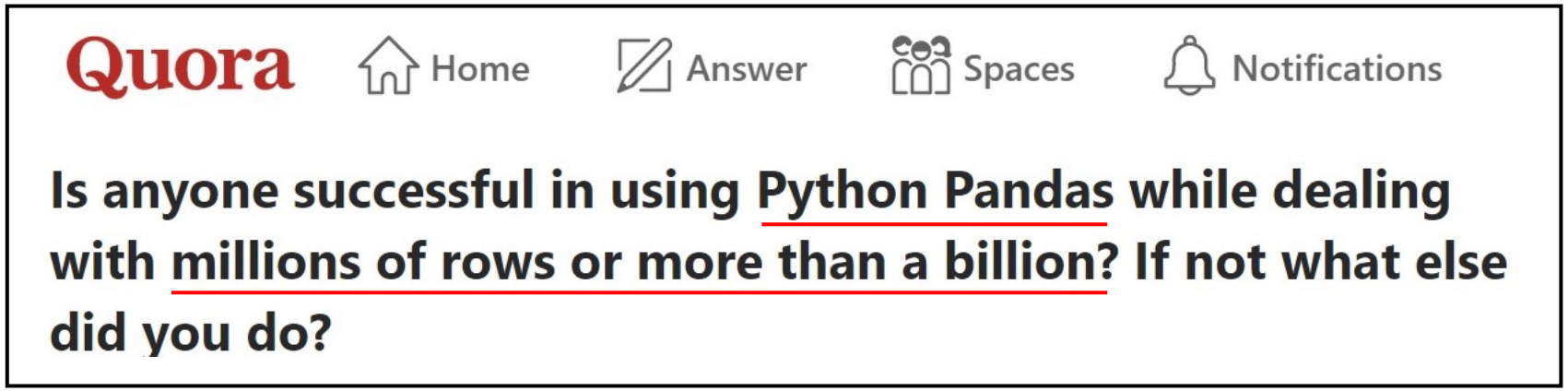

➢Expensive solution: overprovision memory for peak usage.

Recent Far-Memory Systems

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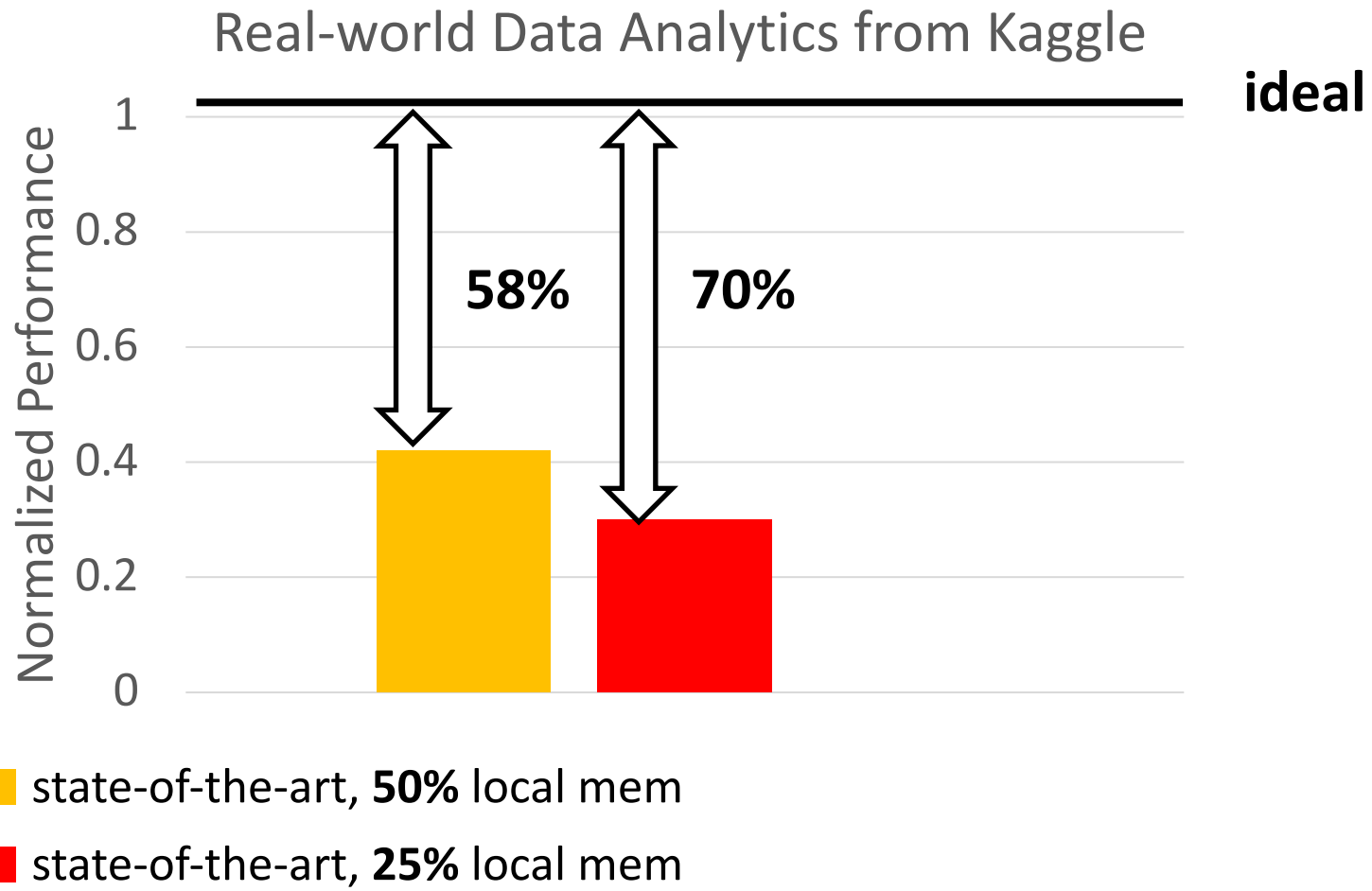
➢Built on top of **OS paging (swap)**.

Does OS-Paging Systems Perform Well?



Why OS-Paging Systems Suffer?

- Goal: transparent, no app code modification.

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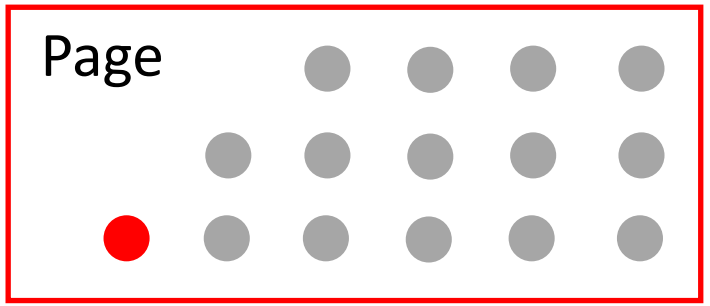
- Require to use OS to manage virtual memory pages.
  - Semantic gap.
  - High kernel overheads.

Semantic Gap (in Paging Systems)

- Page granularity. Example: R/W amplification.



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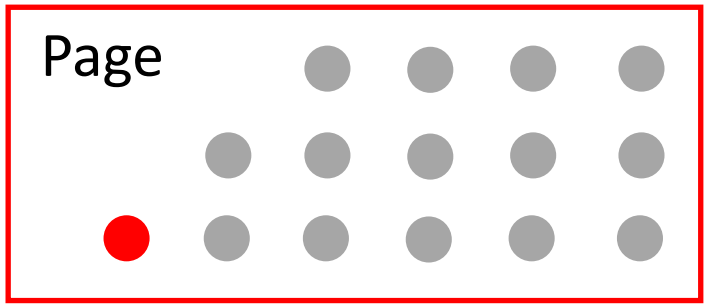

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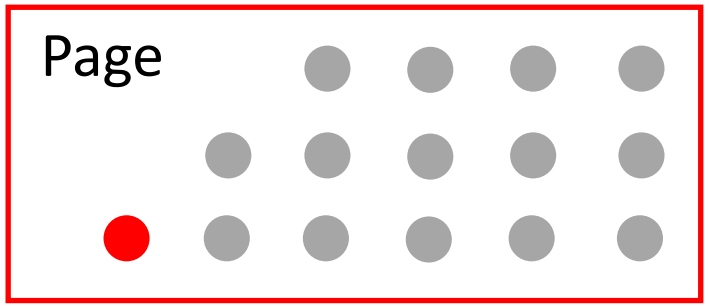

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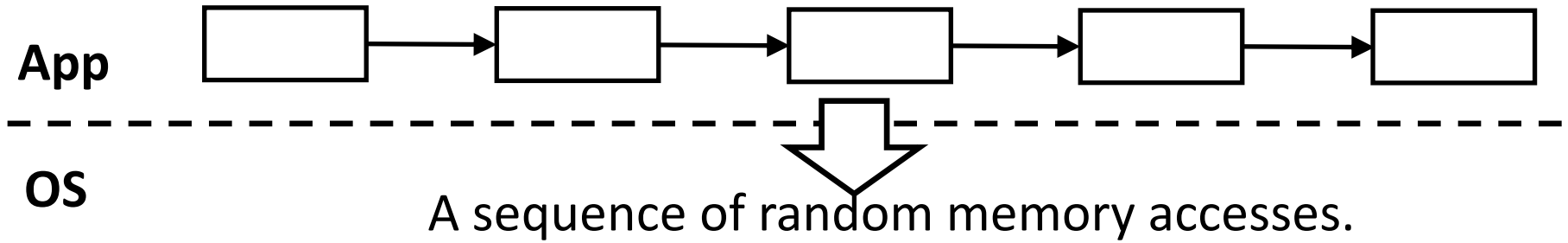

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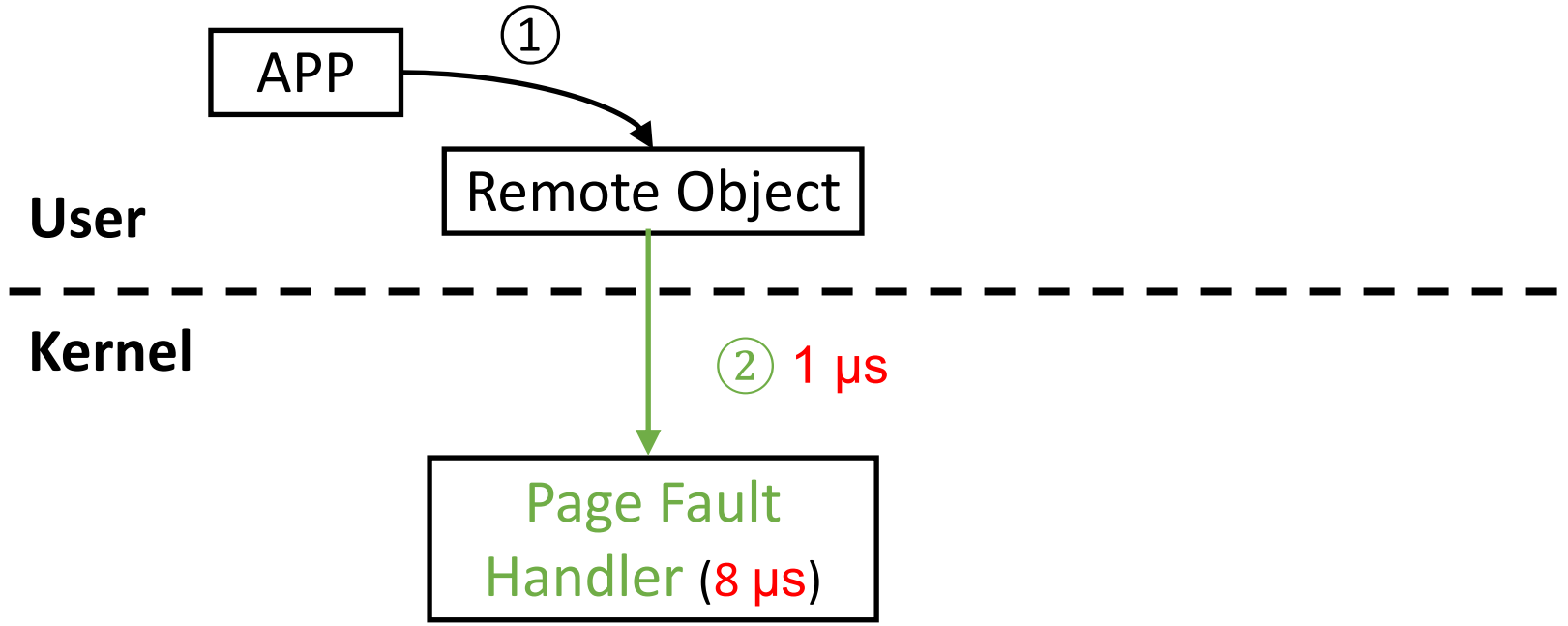

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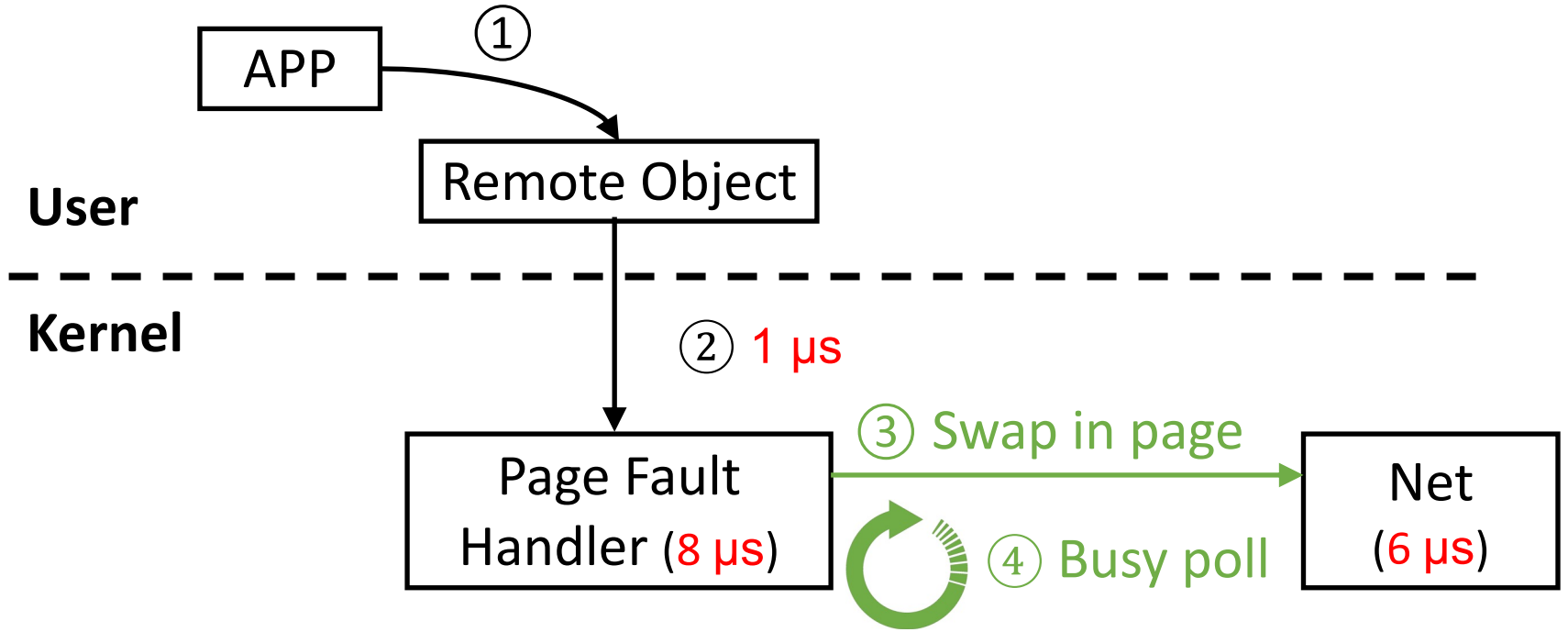
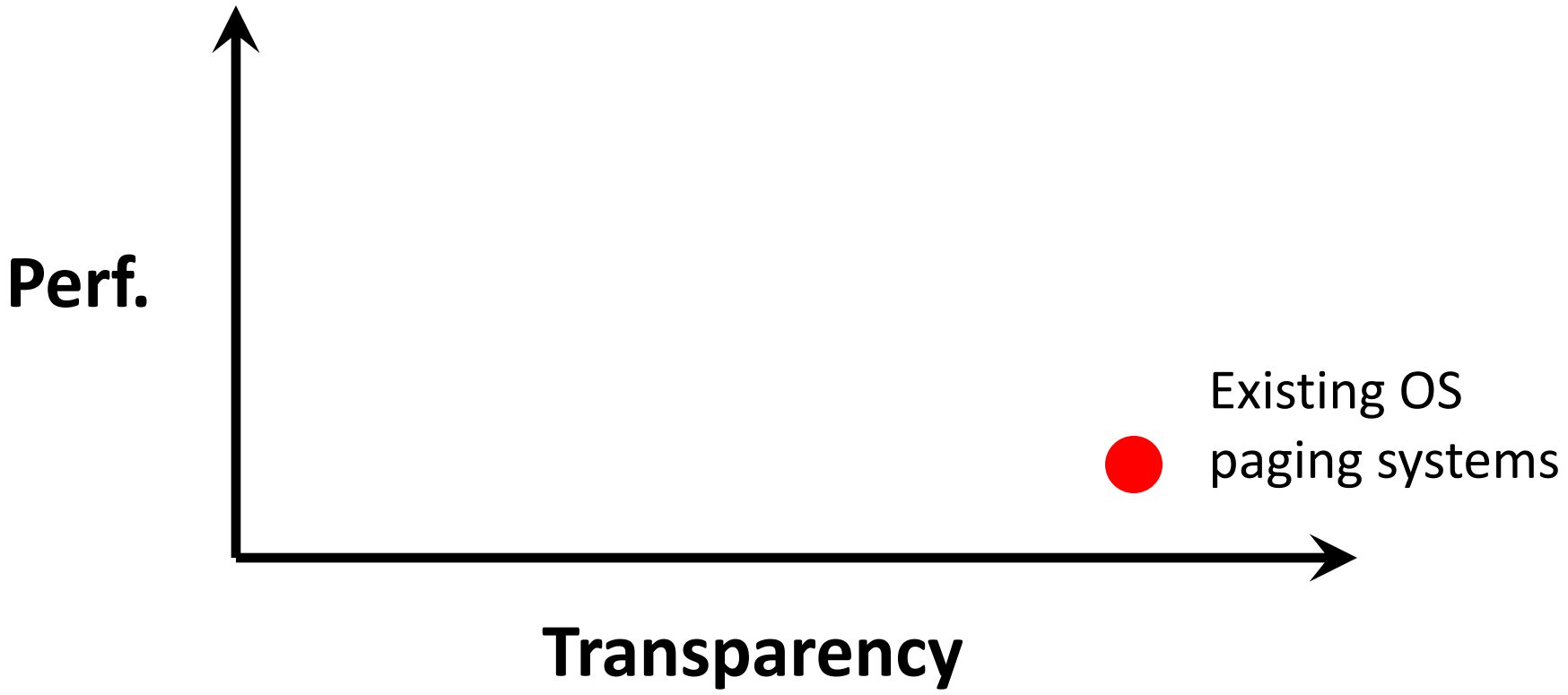
➢Use polling for in-kernel net I/O → burn CPU cycles.



Design Space



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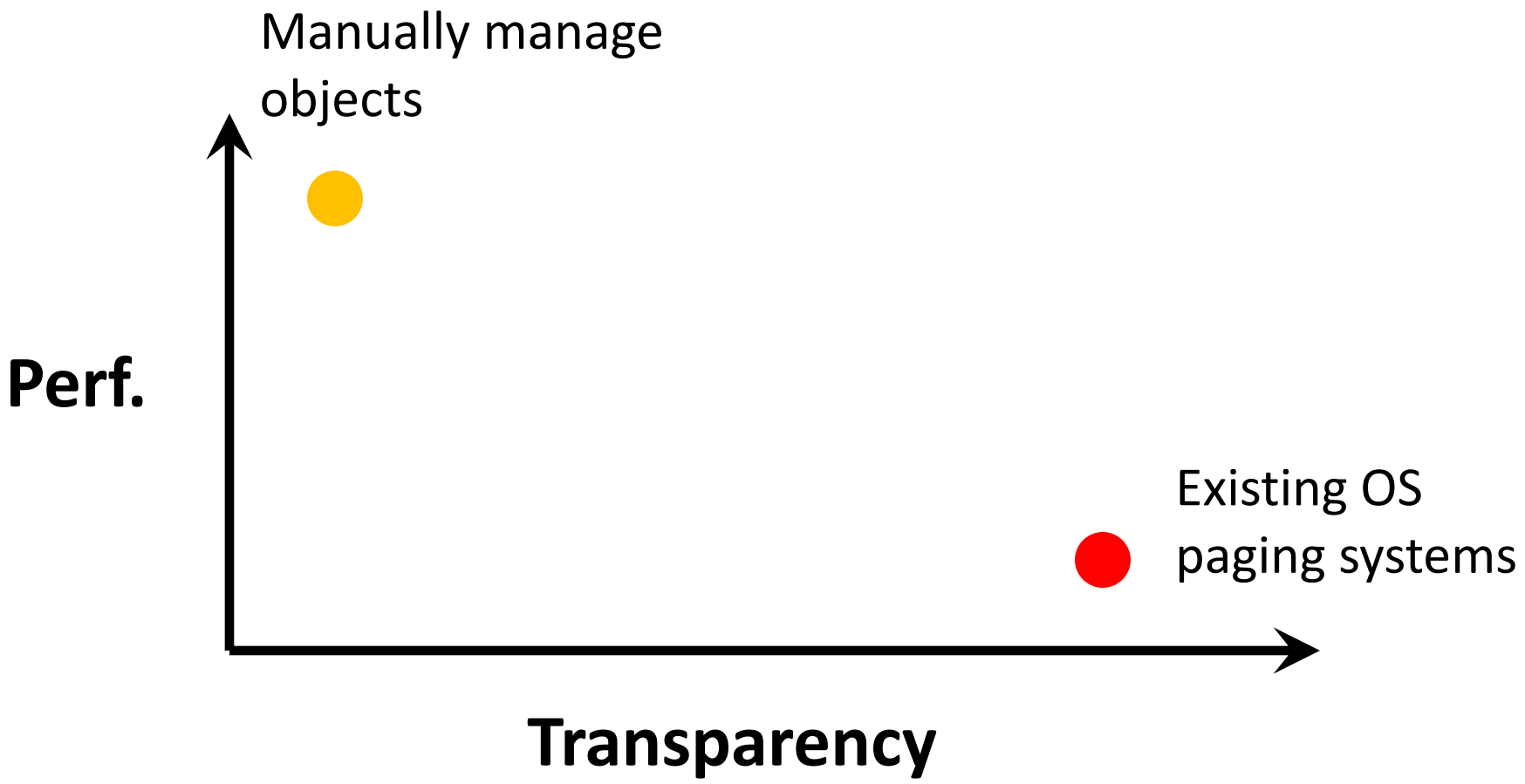

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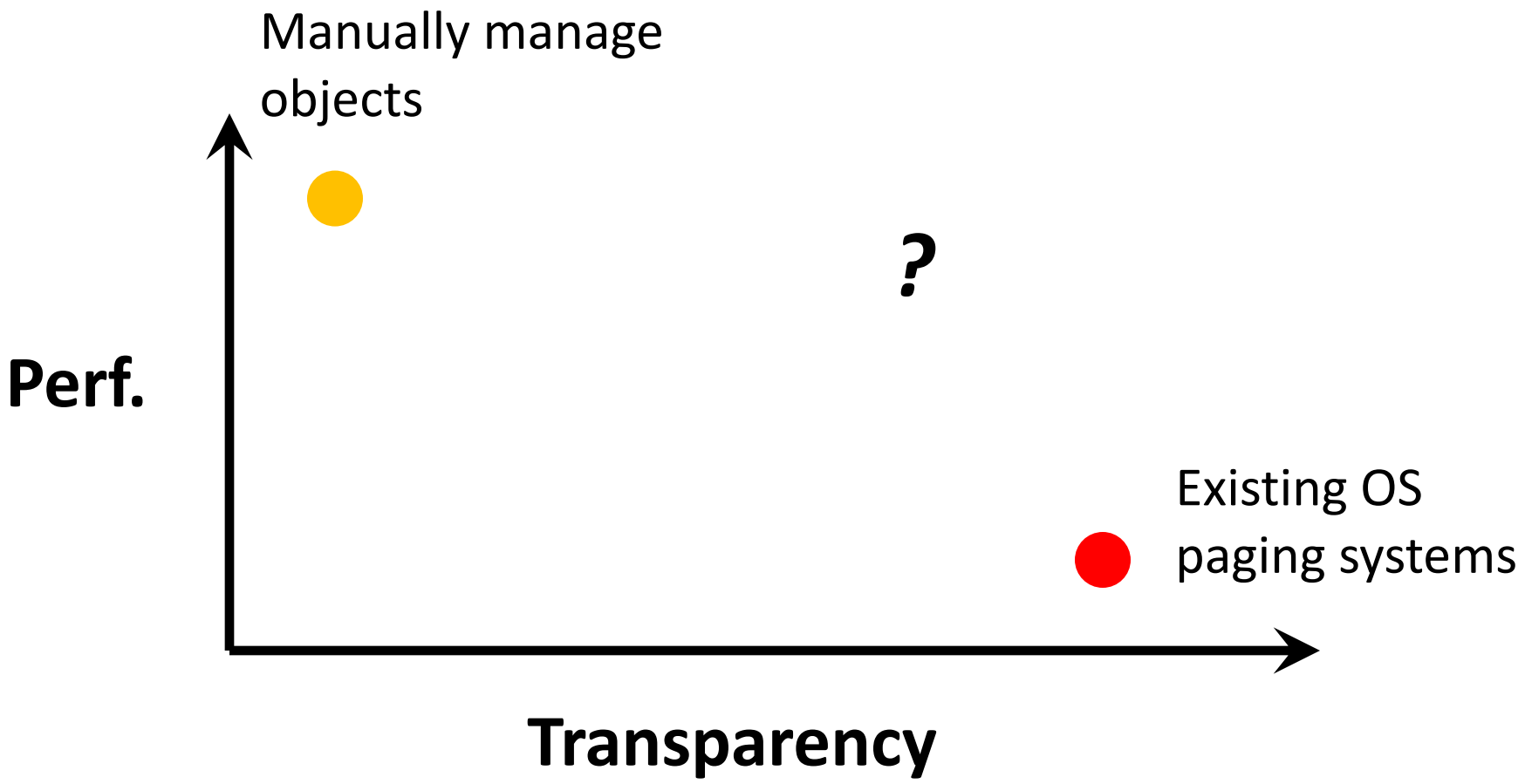

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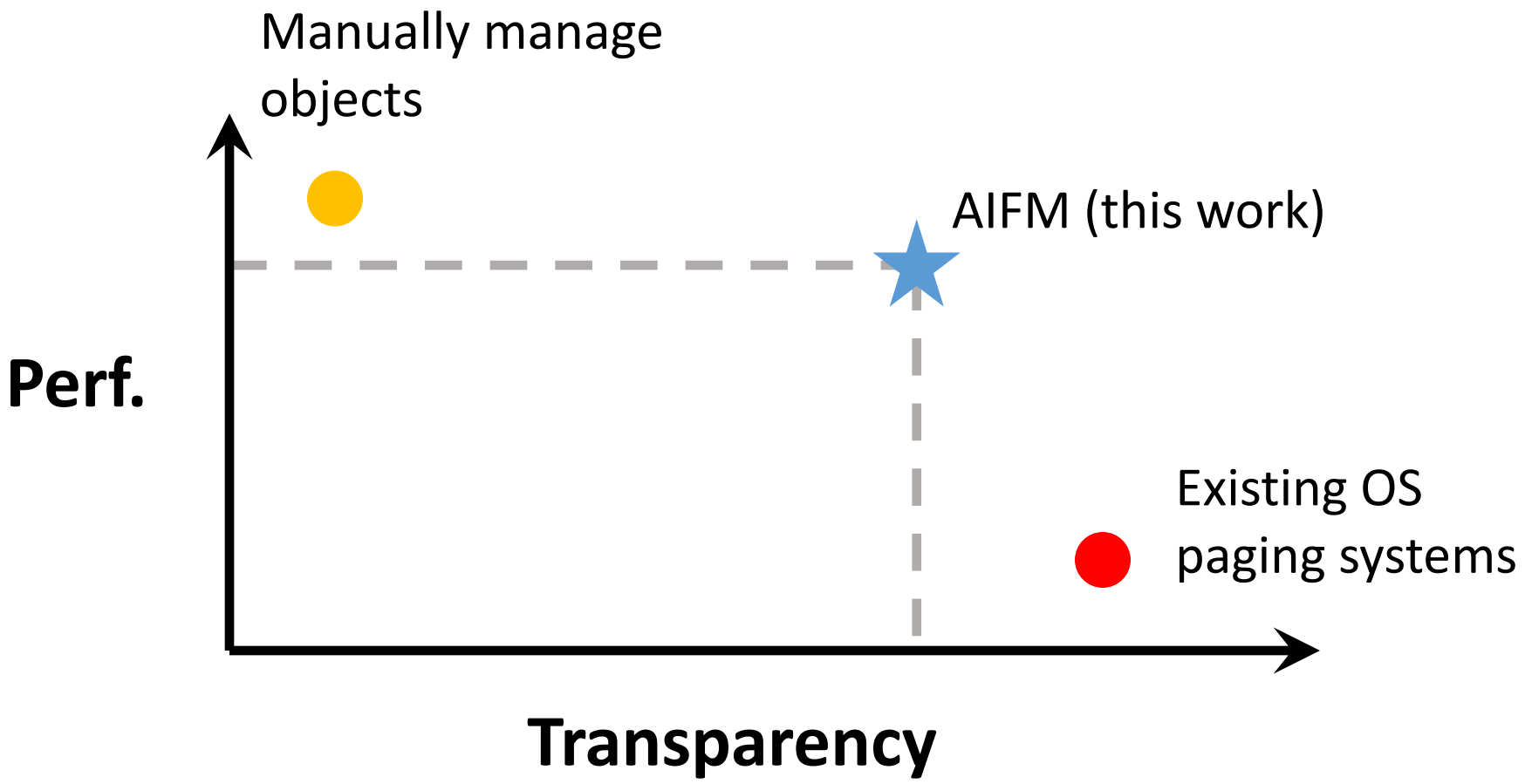
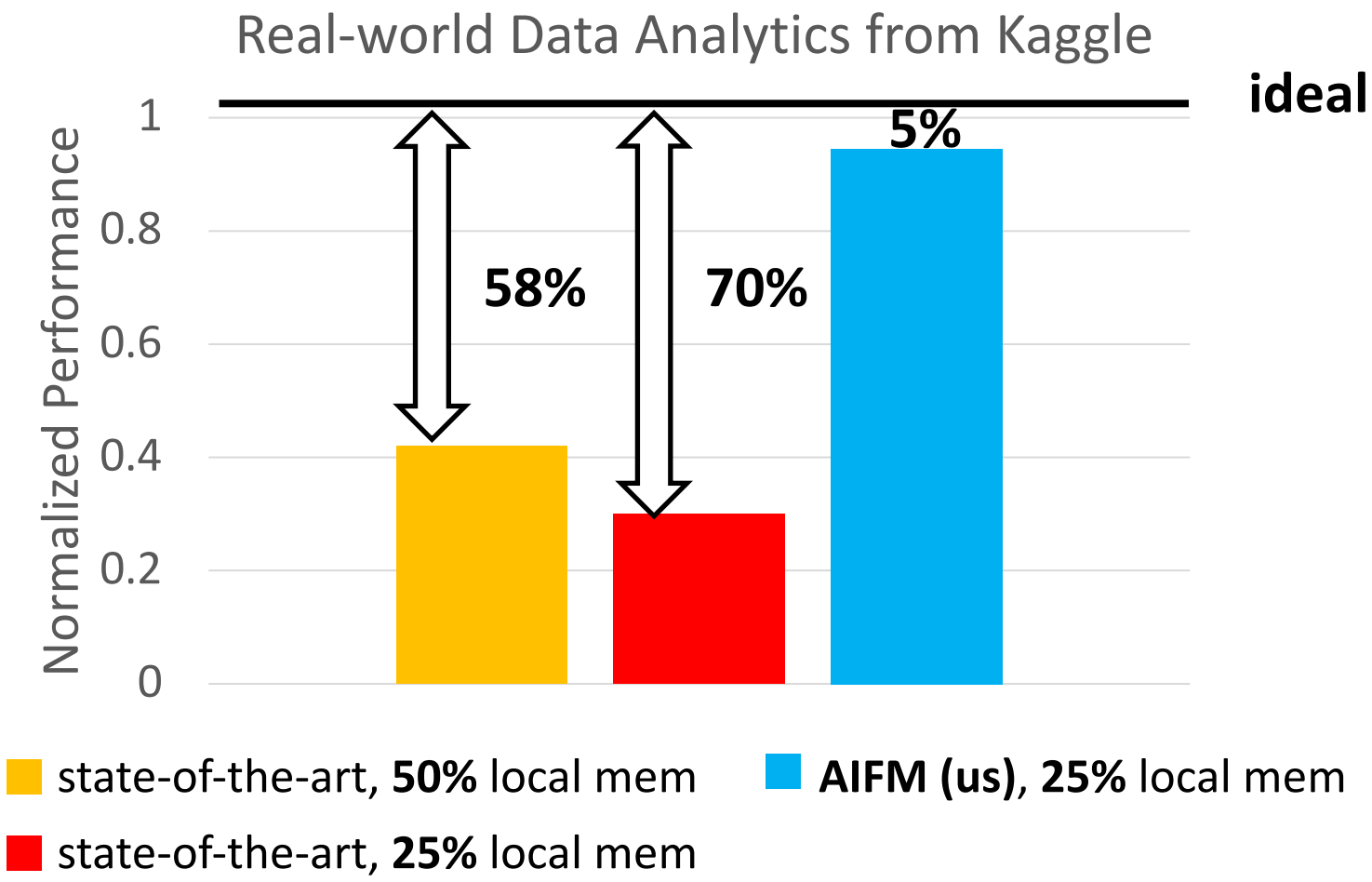


How Does AIFM Perform?



AIFM's Approach

- AIFM: **Application-Integrated** Far Memory.

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- Semantic gap
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	• Userspace runtime that swaps in/out objs

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AIFM in Action

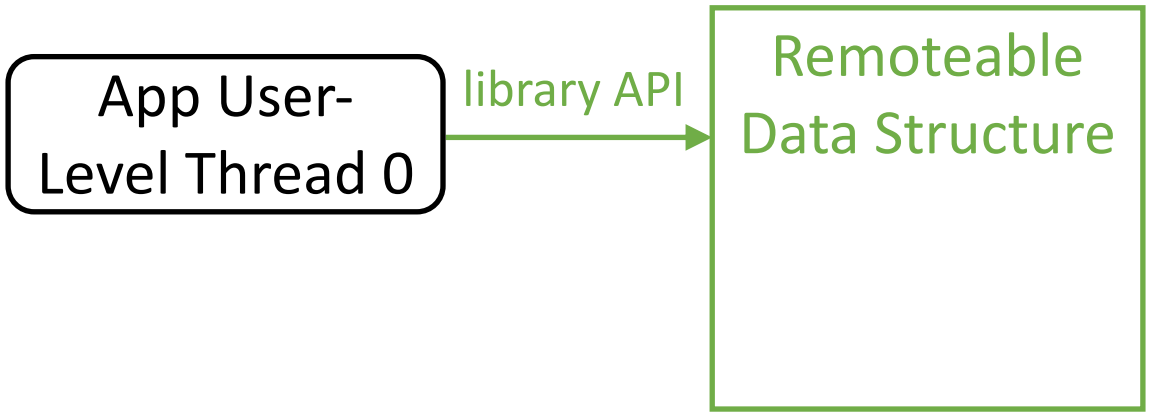
App User-Level Thread 0

Local Memory

Far Memory

1. Remoteable Data Structure Library

- Solved challenge: semantic gap.



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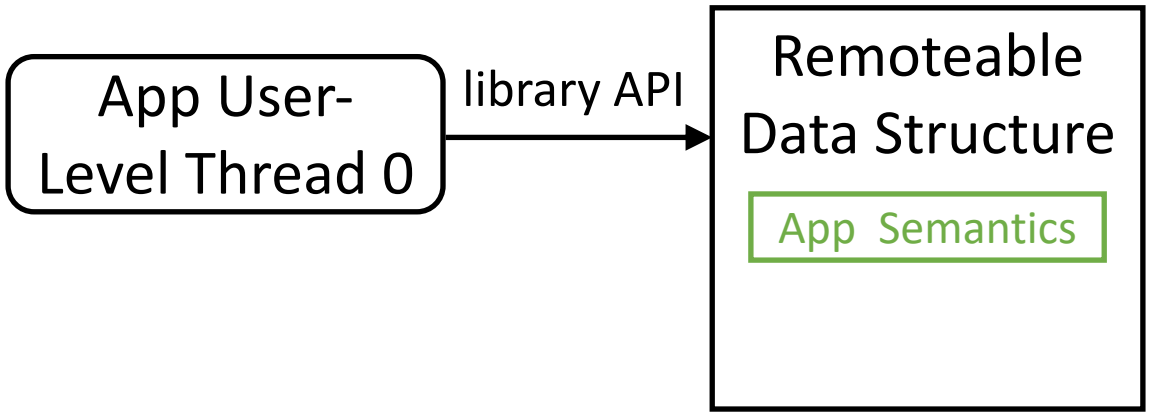

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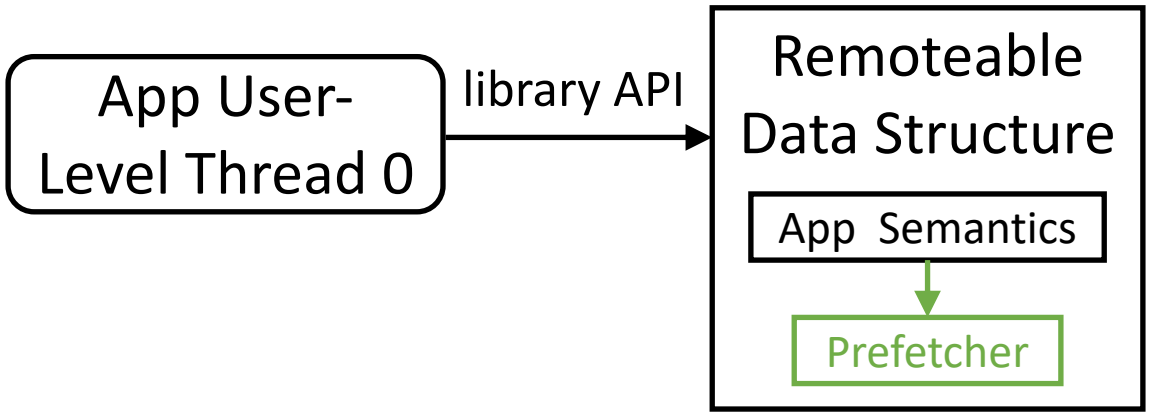

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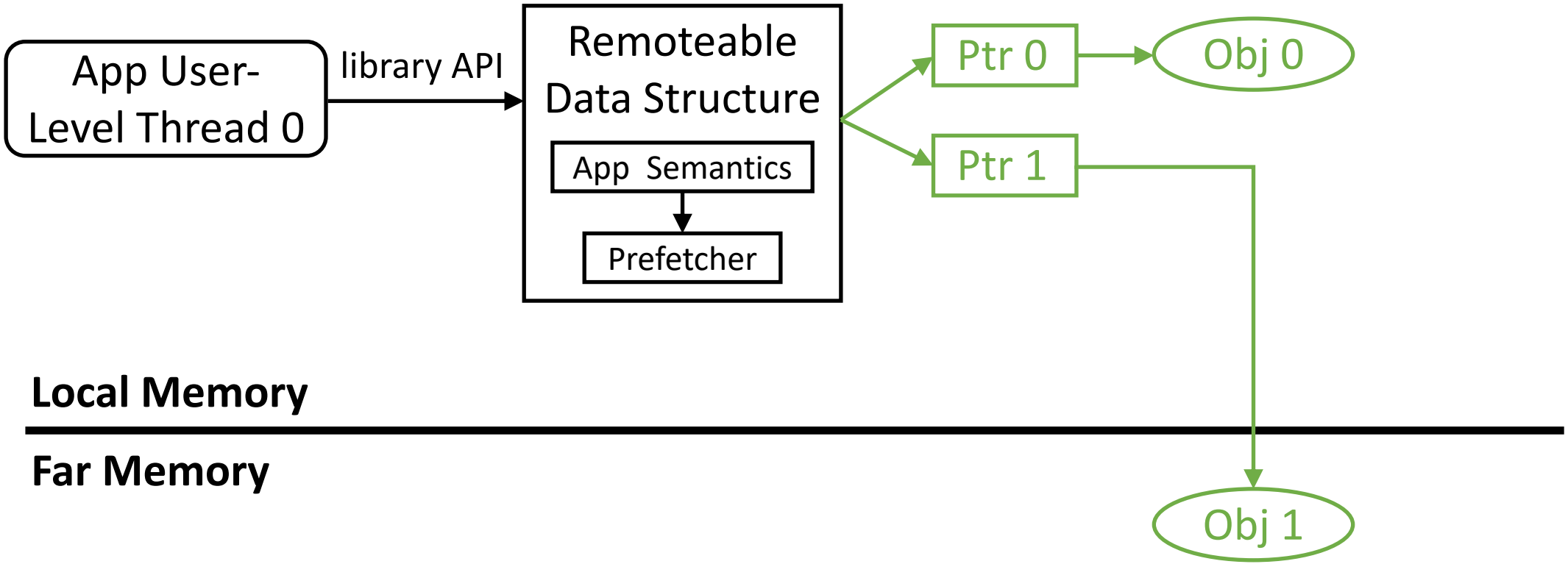

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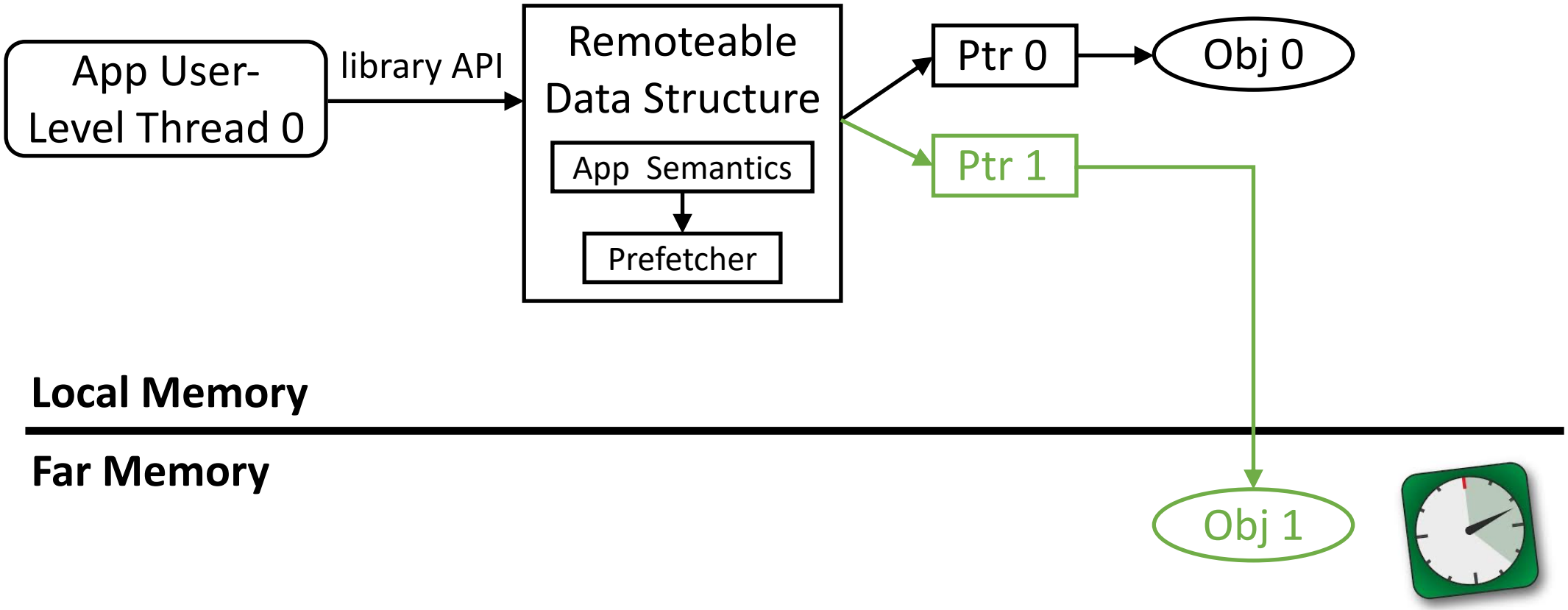

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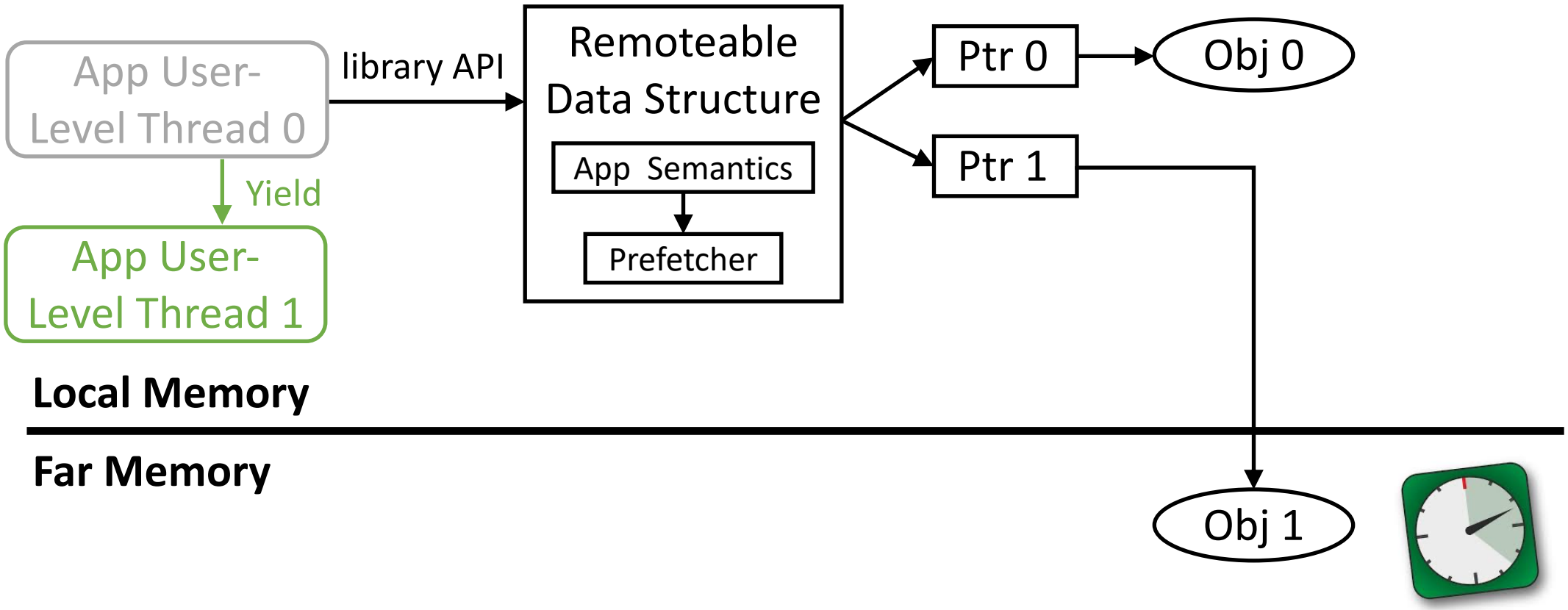

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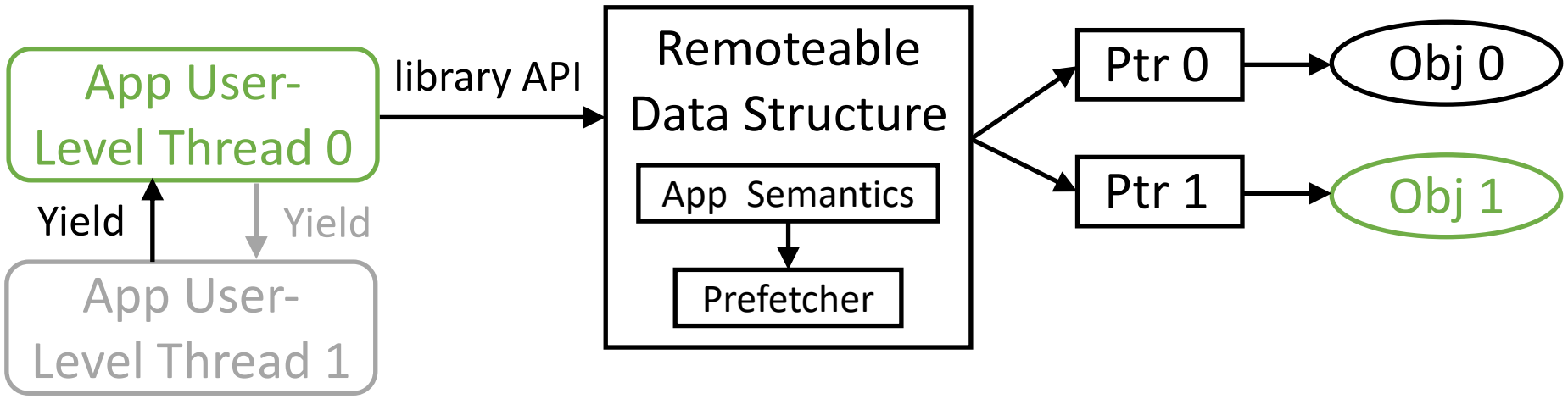

3. Pauseless Evacuator

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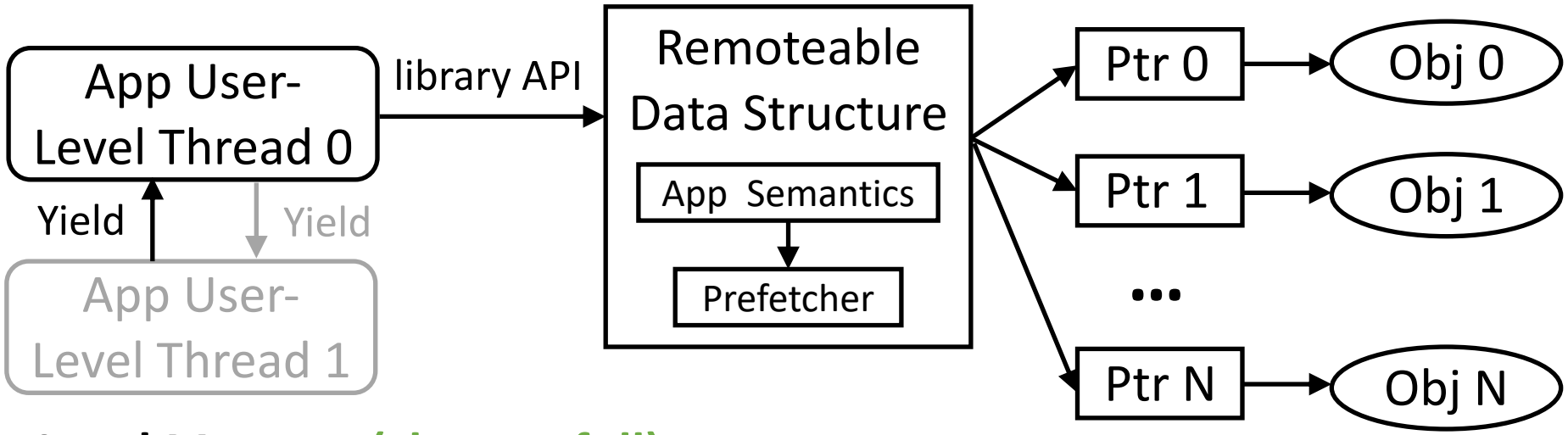

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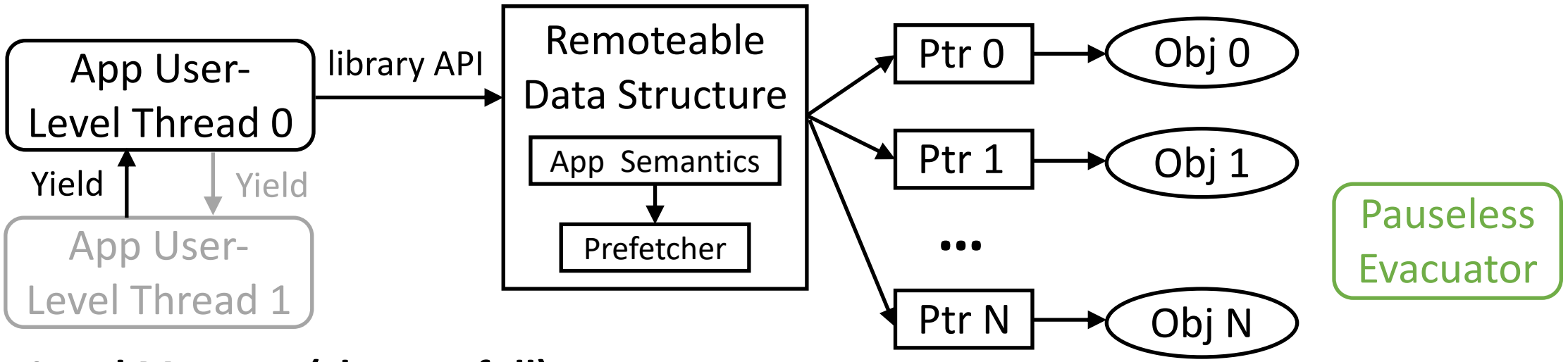

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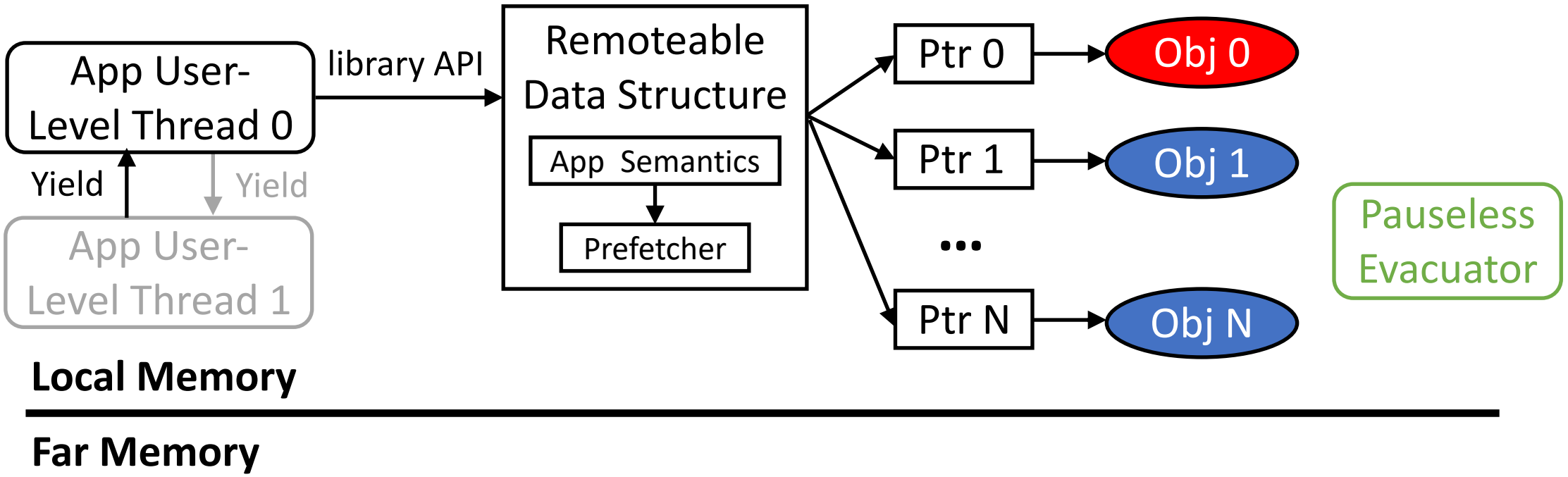

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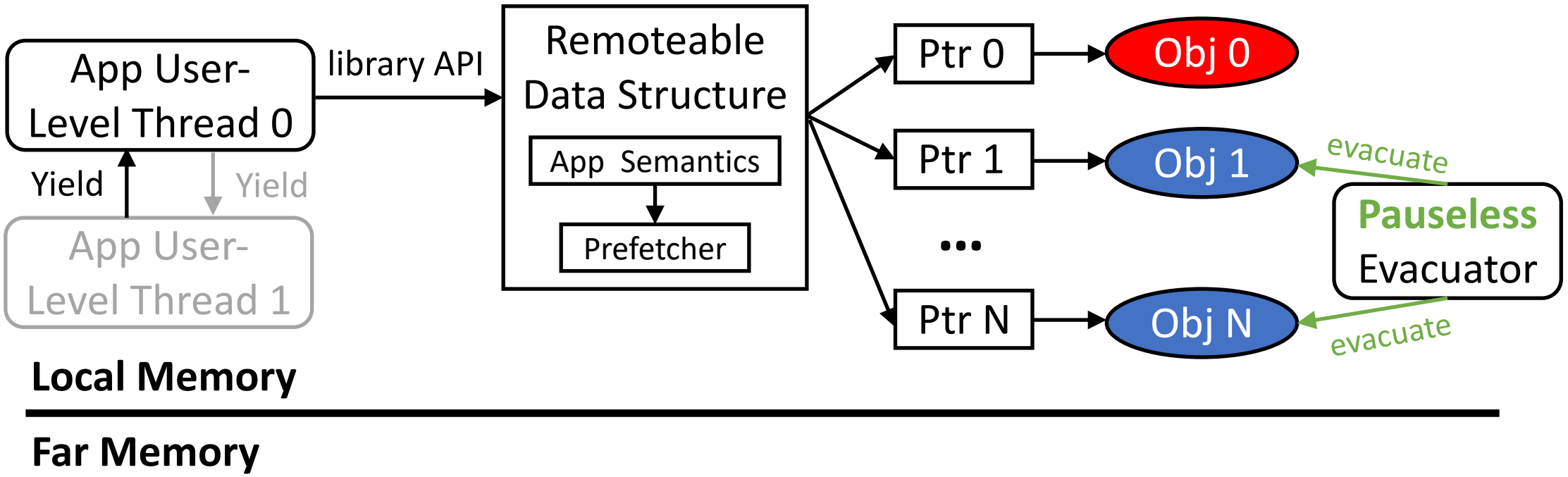

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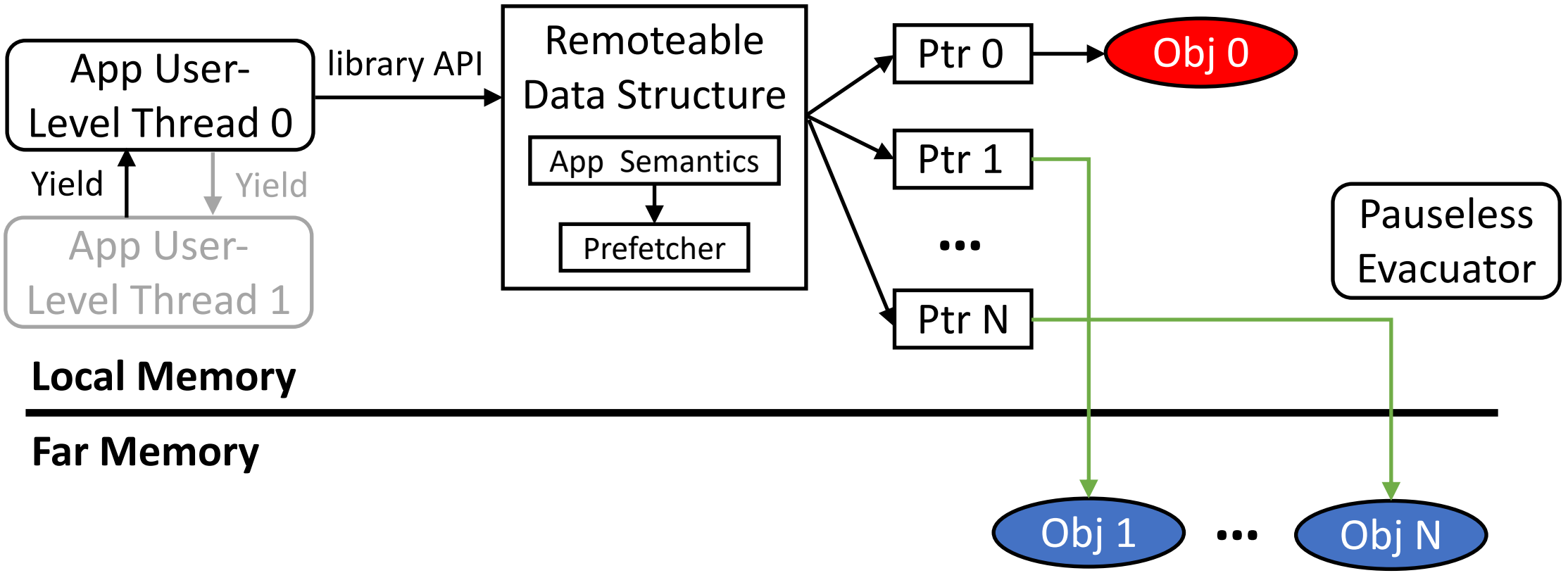

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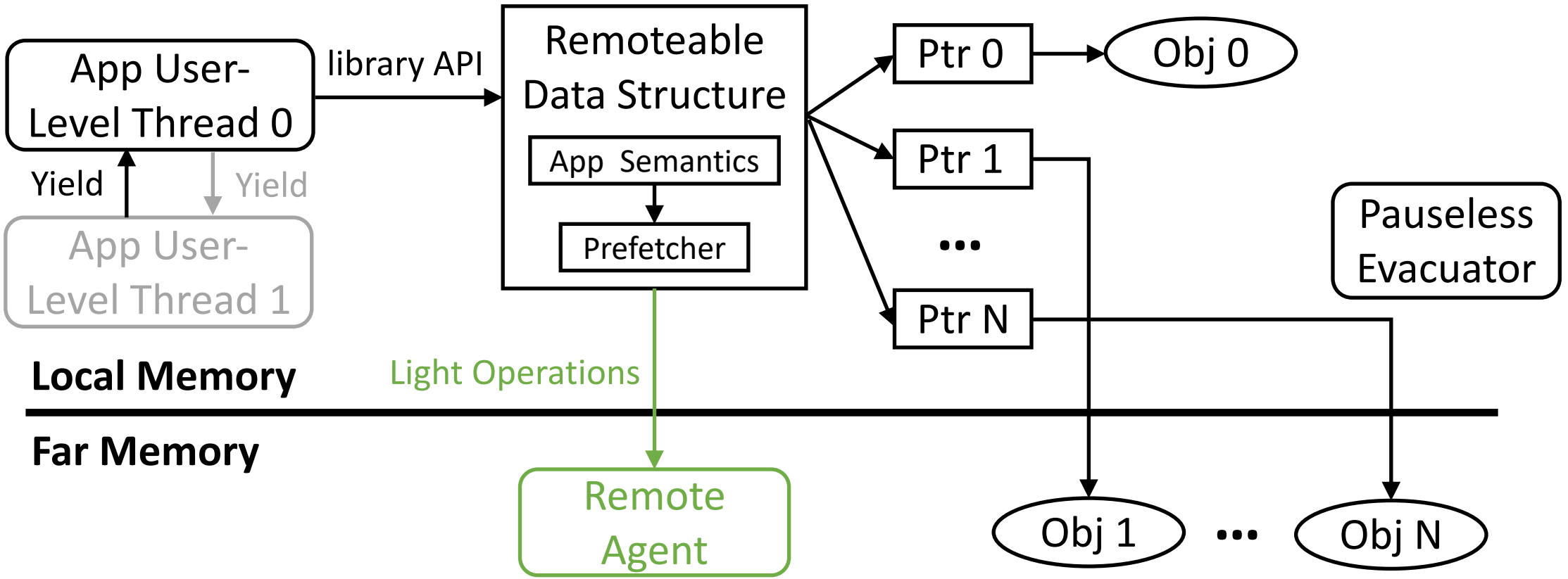

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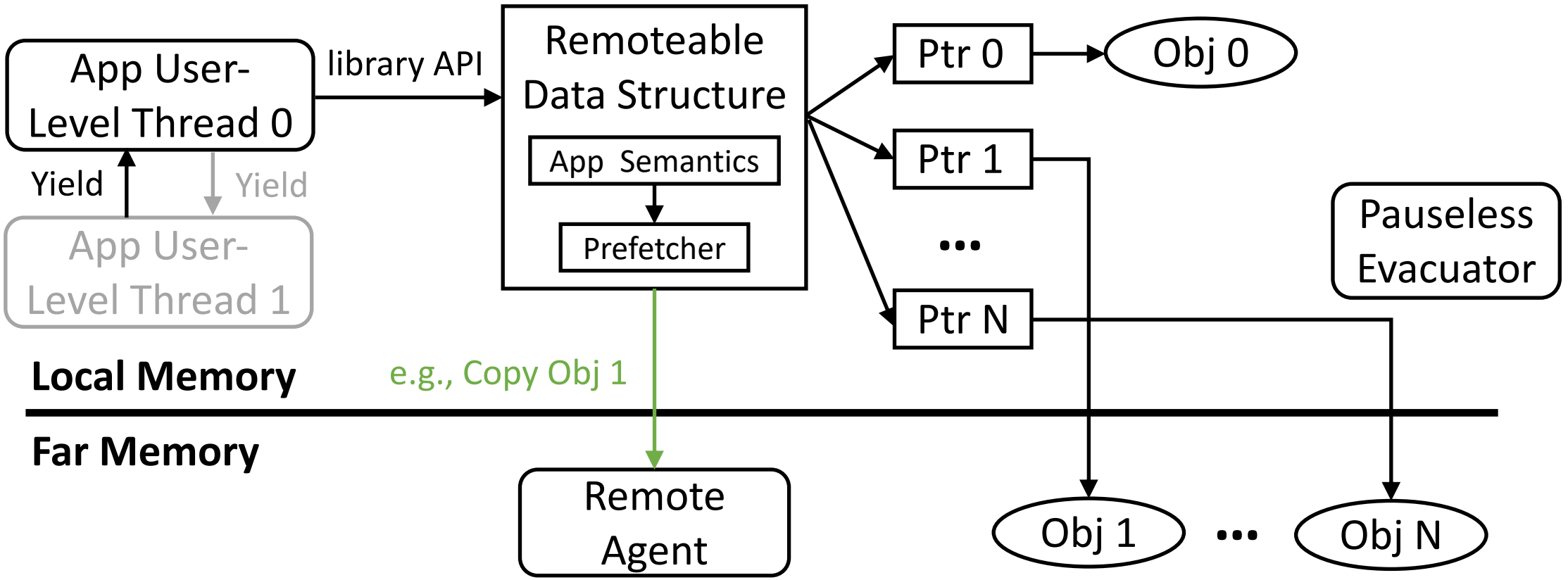

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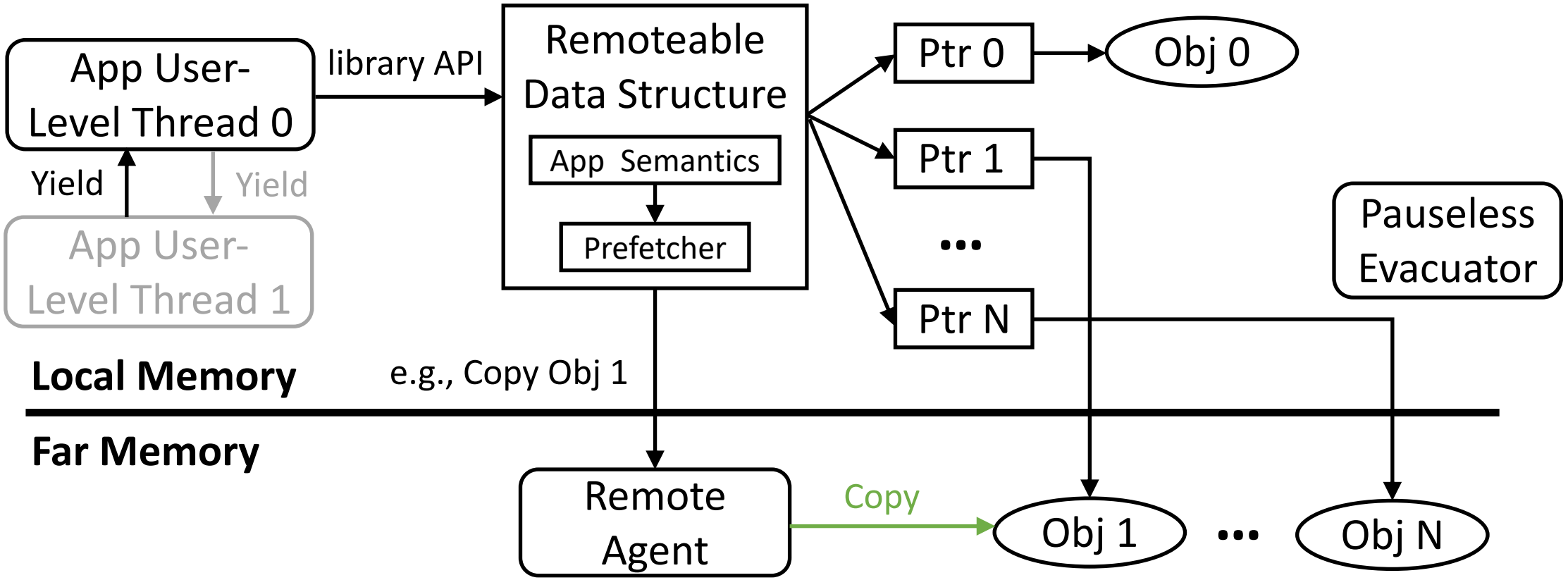

Sample Code

```
std::unordered_map<key_t, int> hashtable;
std::array<LargeData> arr;

LargeData foo(std::list<key_t> &keys_list) {
    int sum = 0;
    for (auto key : keys_list) {

        sum += hashtable.at(key);
    }

    LargeData ret = arr.at(sum);
    return ret;
}
```

Sample Code

```
RemHashTable<key_t, int> hashtable;
RemArray<LargeData> arr;

LargeData foo(RemList<key_t> &keys_list) {
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    for (auto key : keys_list) {

        sum += hashtable.at(key);
    }

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LargeData foo(RemList<key_t> &keys_list) {
    int sum = 0;
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        DerefScope scope;
        sum += hashtable.at(key, scope);
    }
    DerefScope scope;
    LargeData ret = arr.at(sum, scope);
    return ret;
}
```

Ensure the objects being accessed will not be moved by the evacuator.

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LargeData foo(RemList<key_t> &keys_list) {
   int sum = 0;
   for (auto key : keys_list) {                    Prefetch list data.
      DerefScope scope;
      sum += hashtable.at(key, scope);
   }
   DerefScope scope;
   LargeData ret = arr.at</*don't cache*/ true>(sum, scope);
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  }
  DerefScope scope;
  LargeData ret = arr.at</*don't cache*/ true>(sum, scope);   Avoid polluting local mem.
  return ret;
}
```

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- Implemented 6 data structures.
  - Array, List, Hashtable, Vector, Stack, and Queue.

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- TCP-based far memory backend.

➢LoC: 6.5K (core runtime) + 5.5K (data structures) + 0.8K (Shenango)

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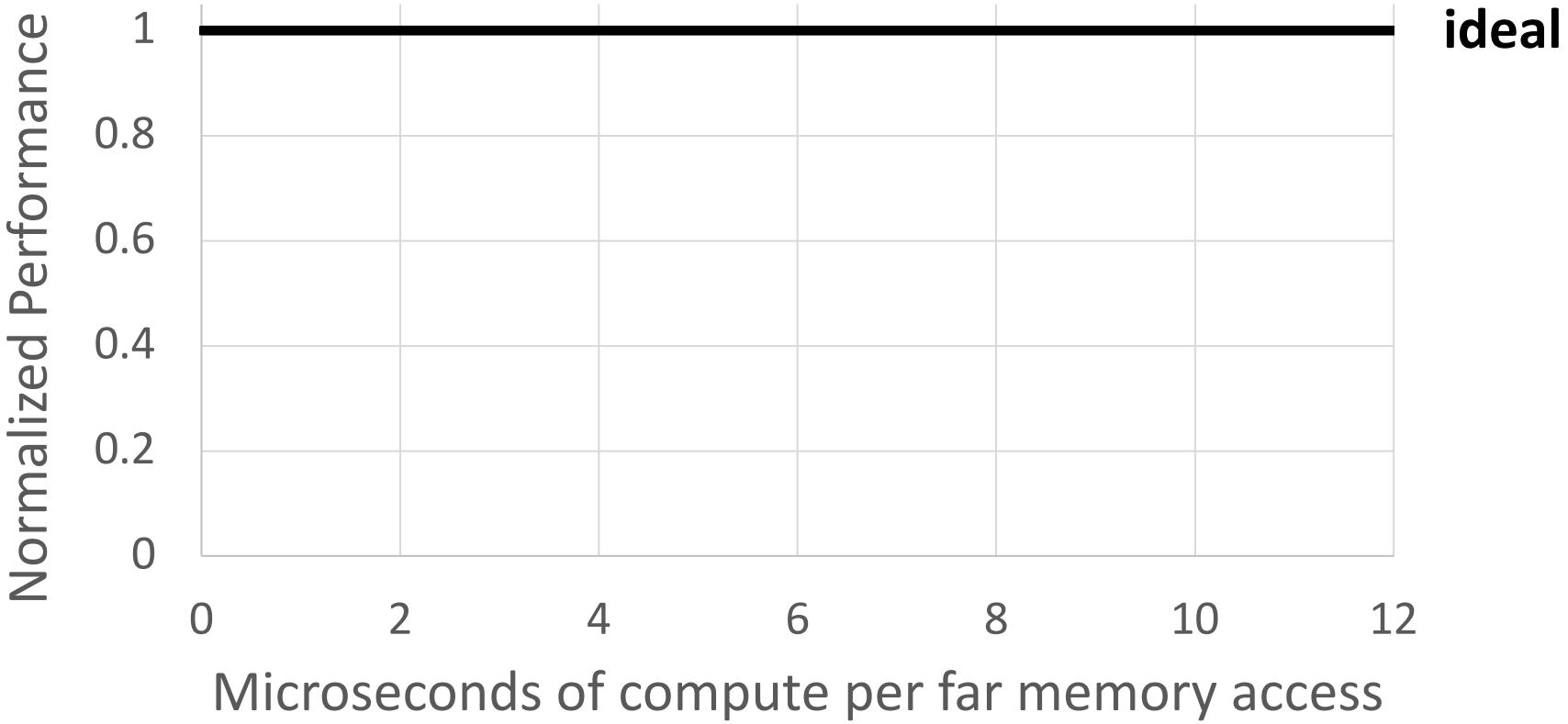
  - ➢… compare to the state-of-the-art paging system, Fastswap [EuroSys' 20]?

Performance on Different Compute Intensities



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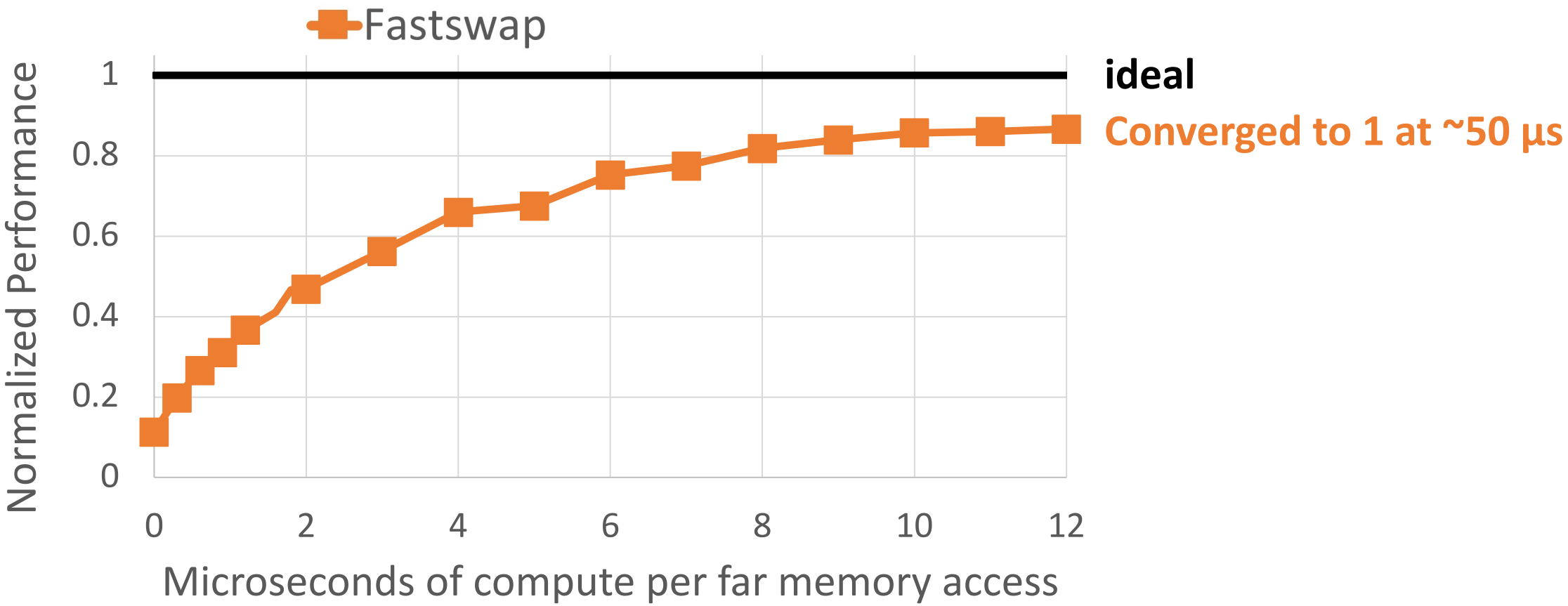

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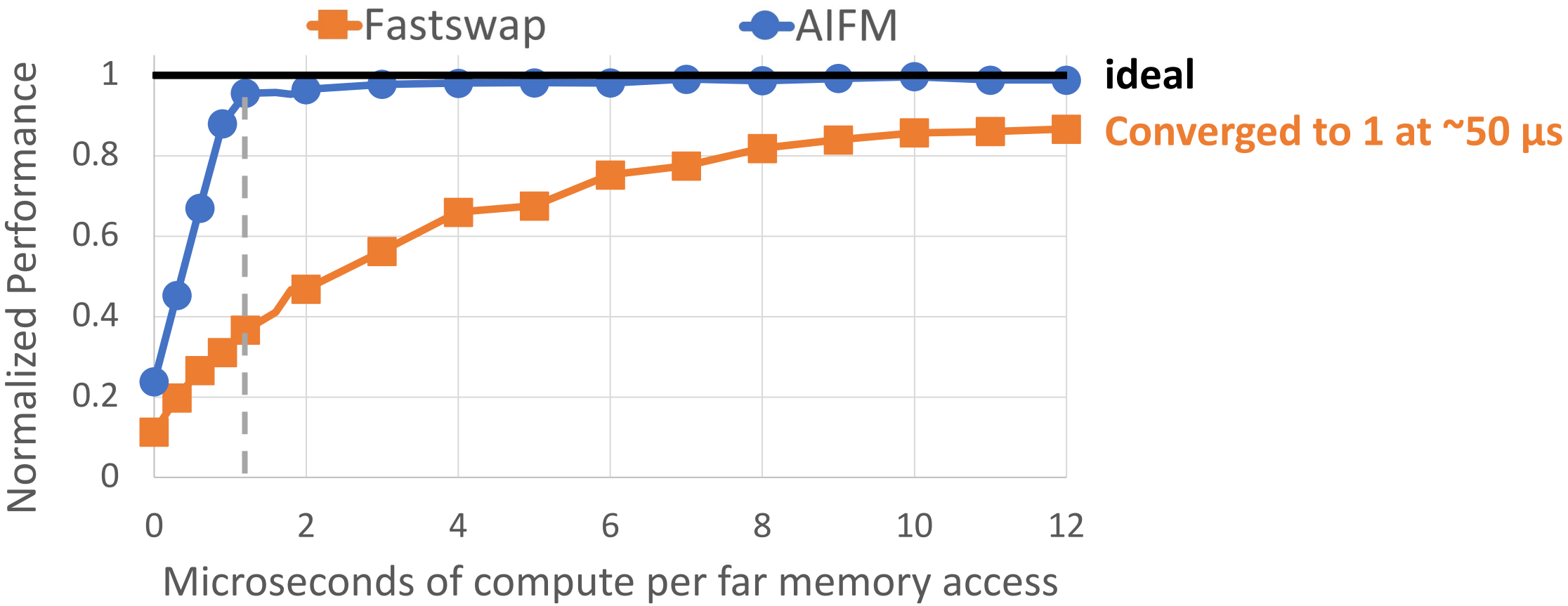

AIFM hides far memory latency with moderate compute.

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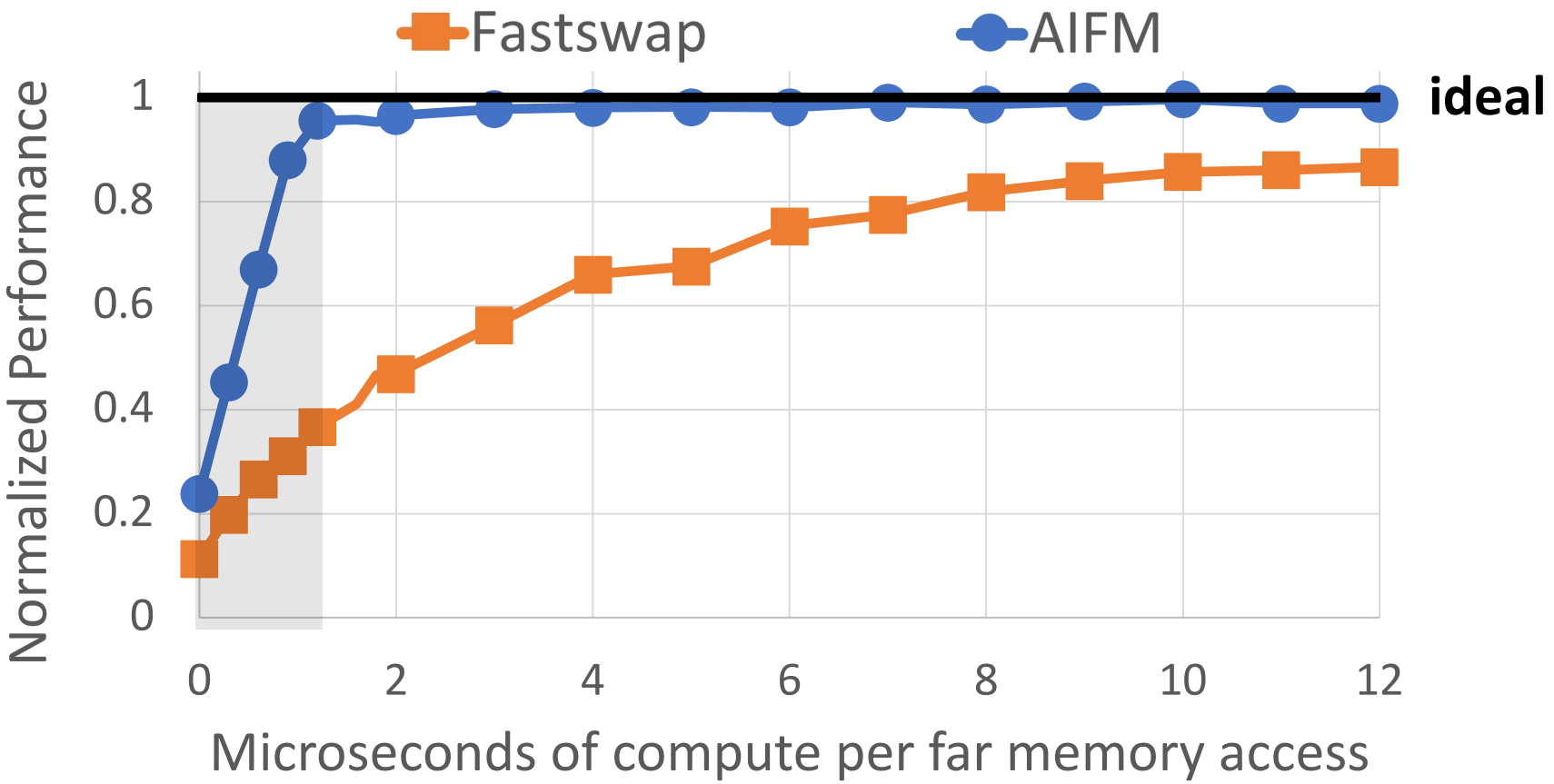

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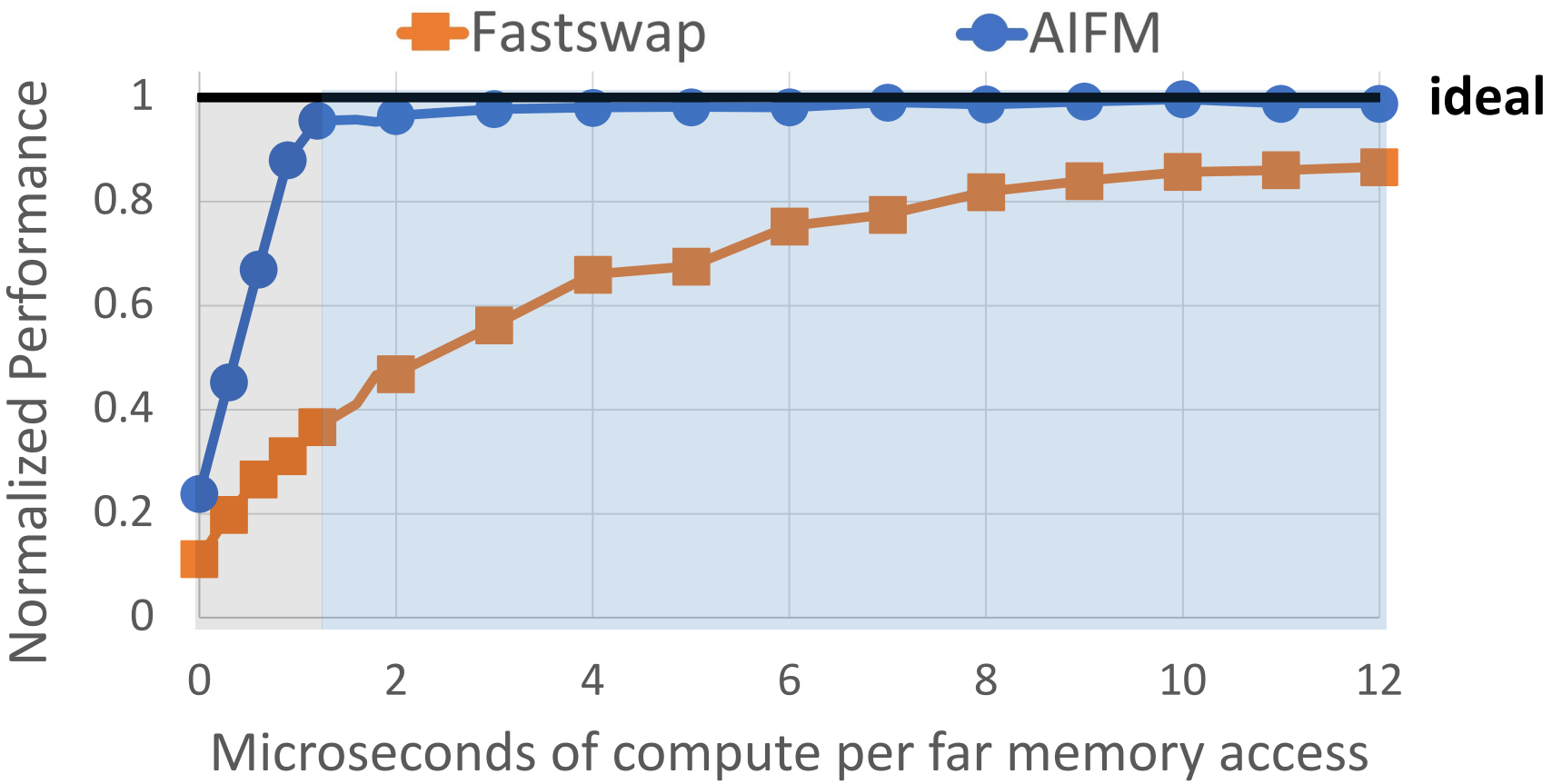

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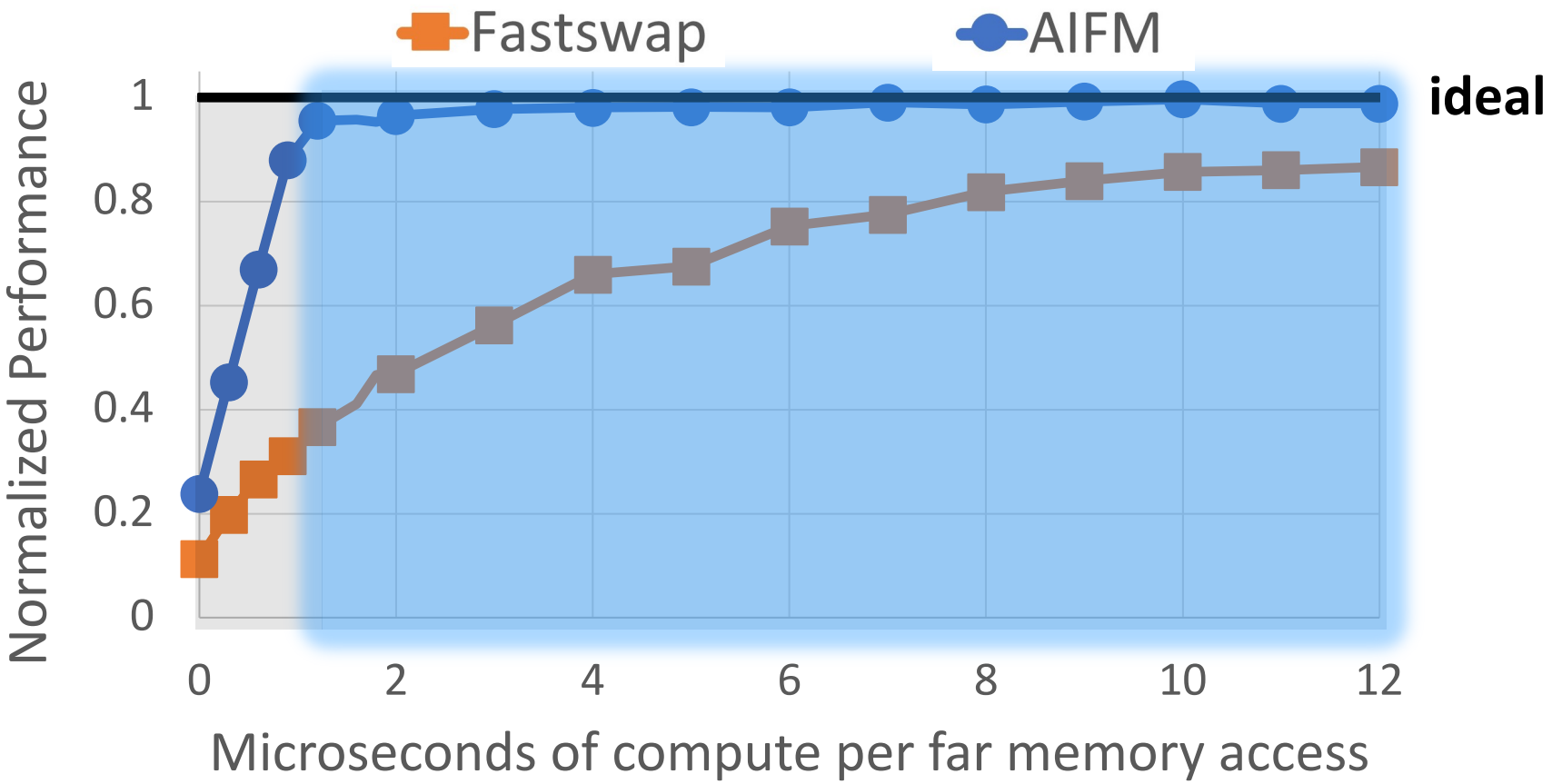
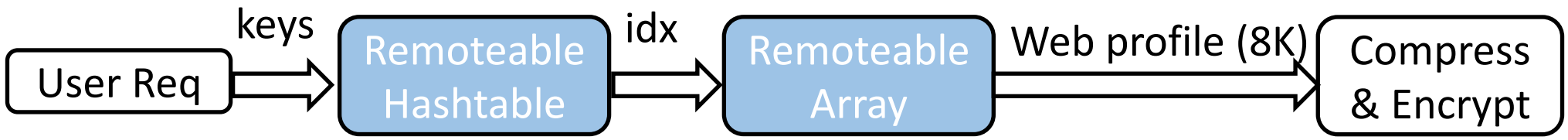


Synthetic Web Frontend



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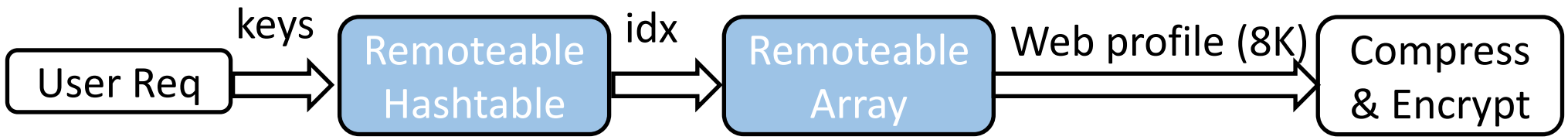
- Object-level caching.



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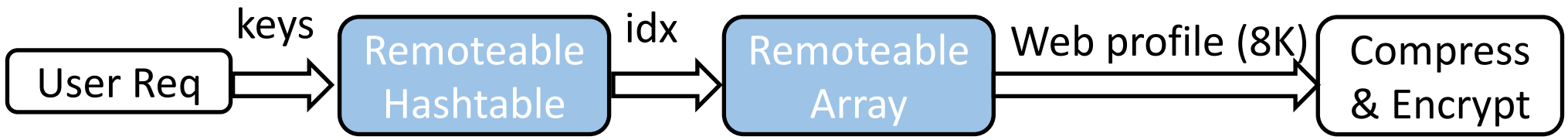

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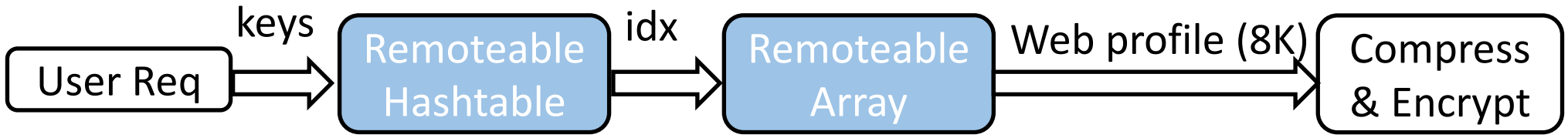

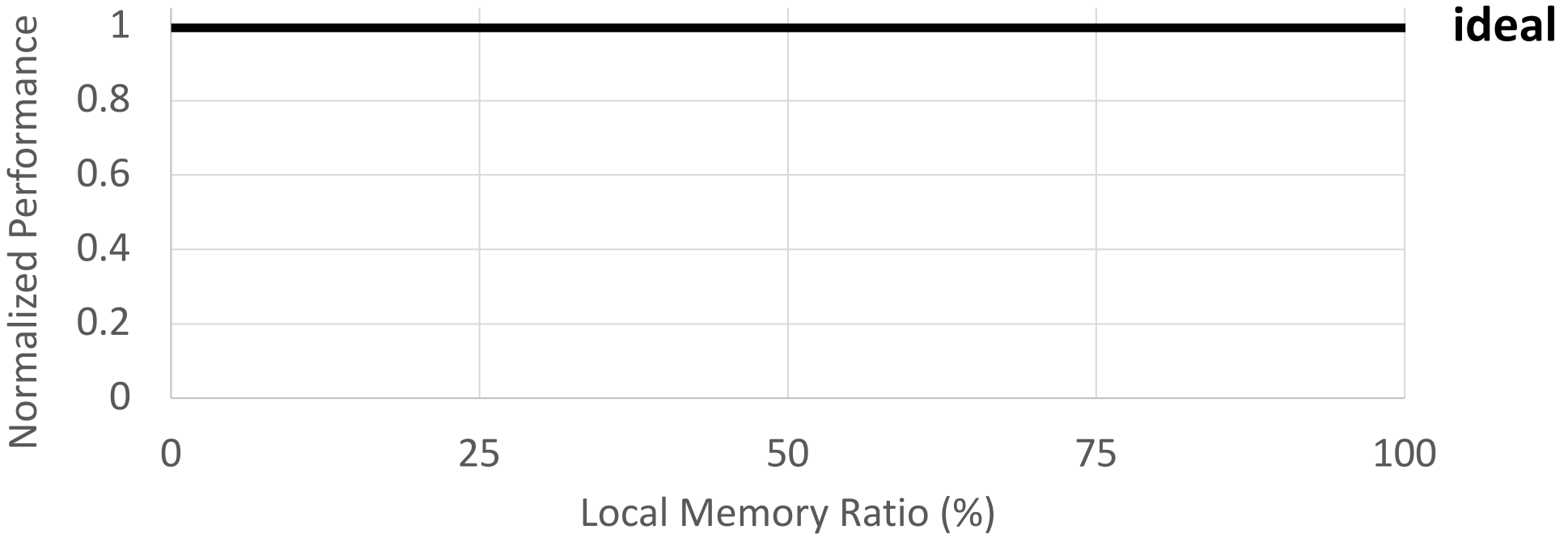

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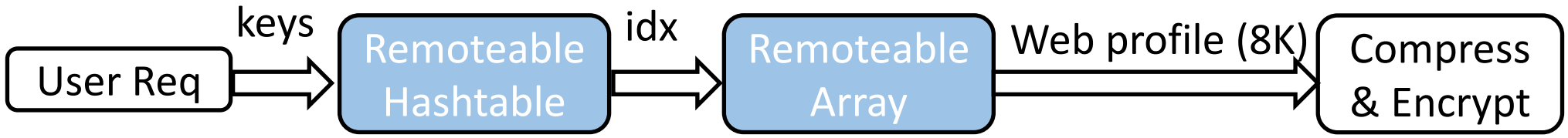

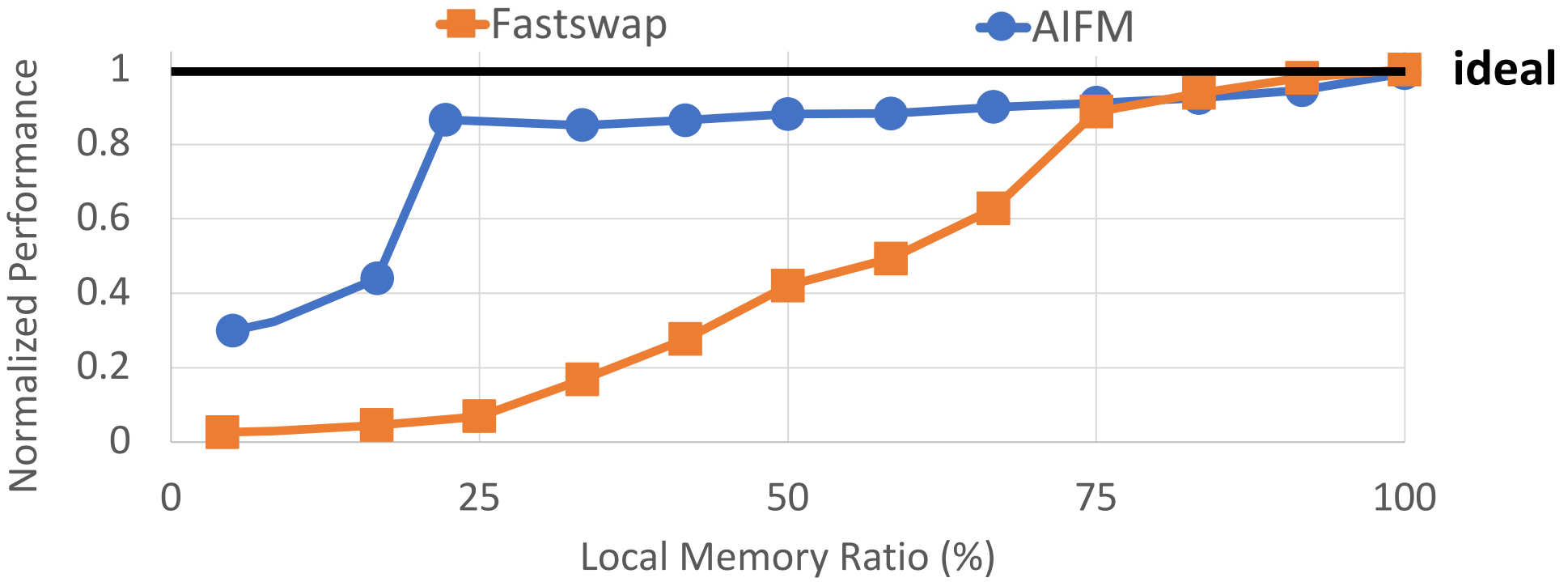

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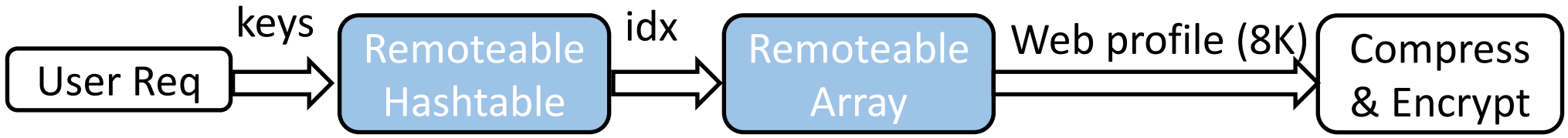

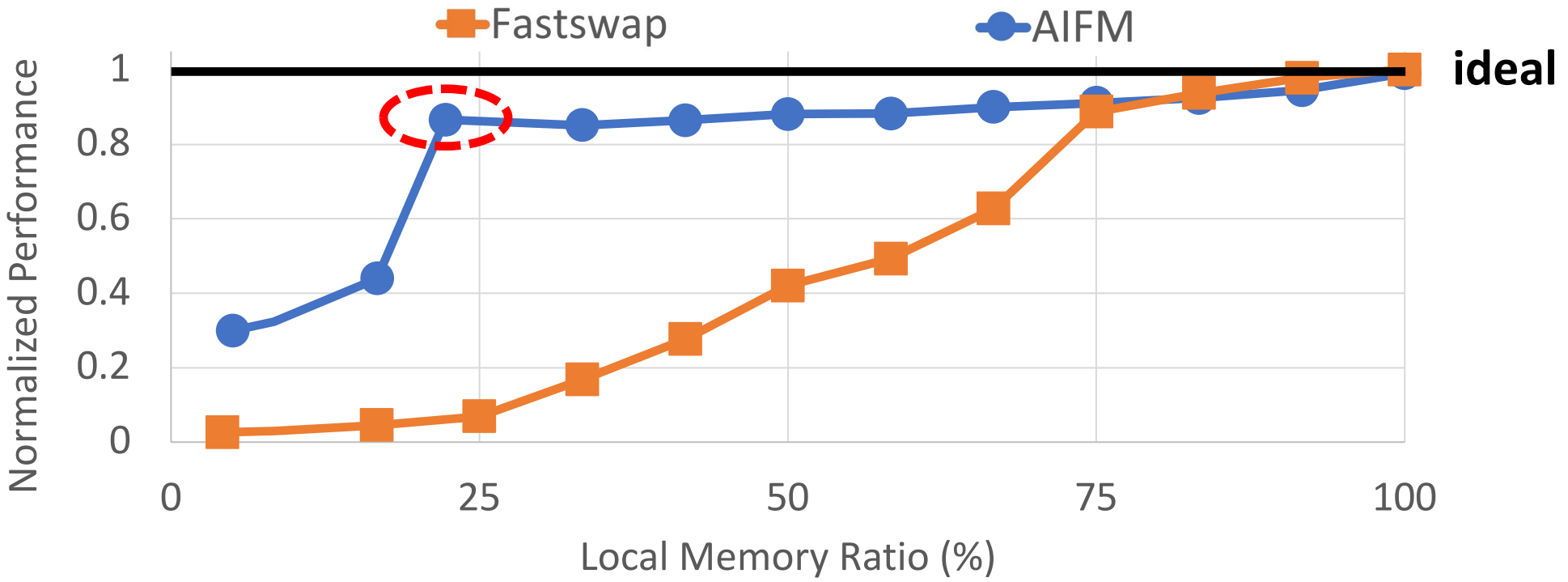

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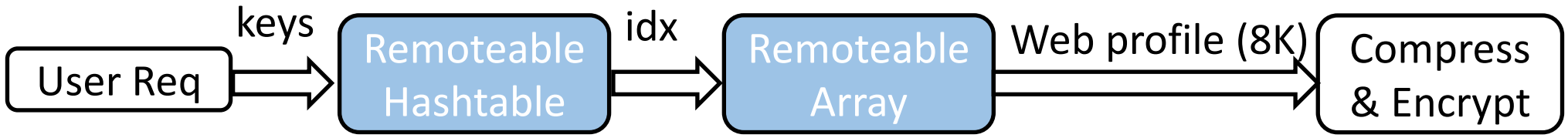

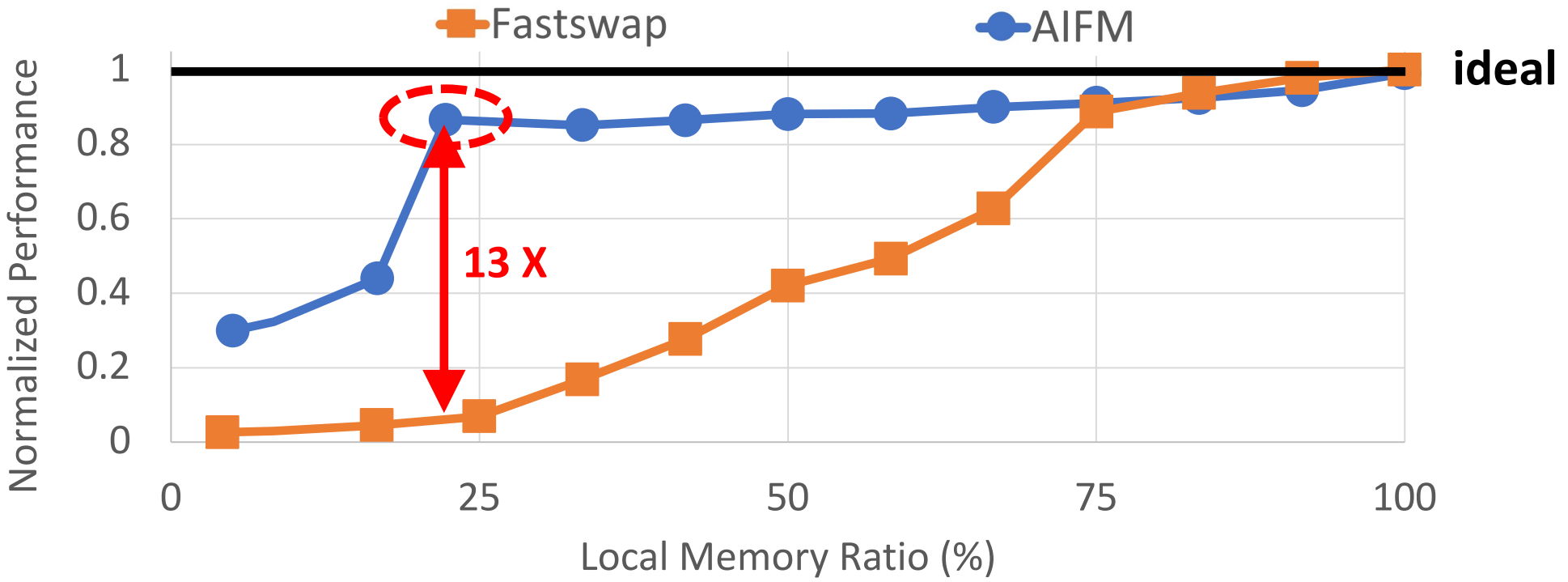

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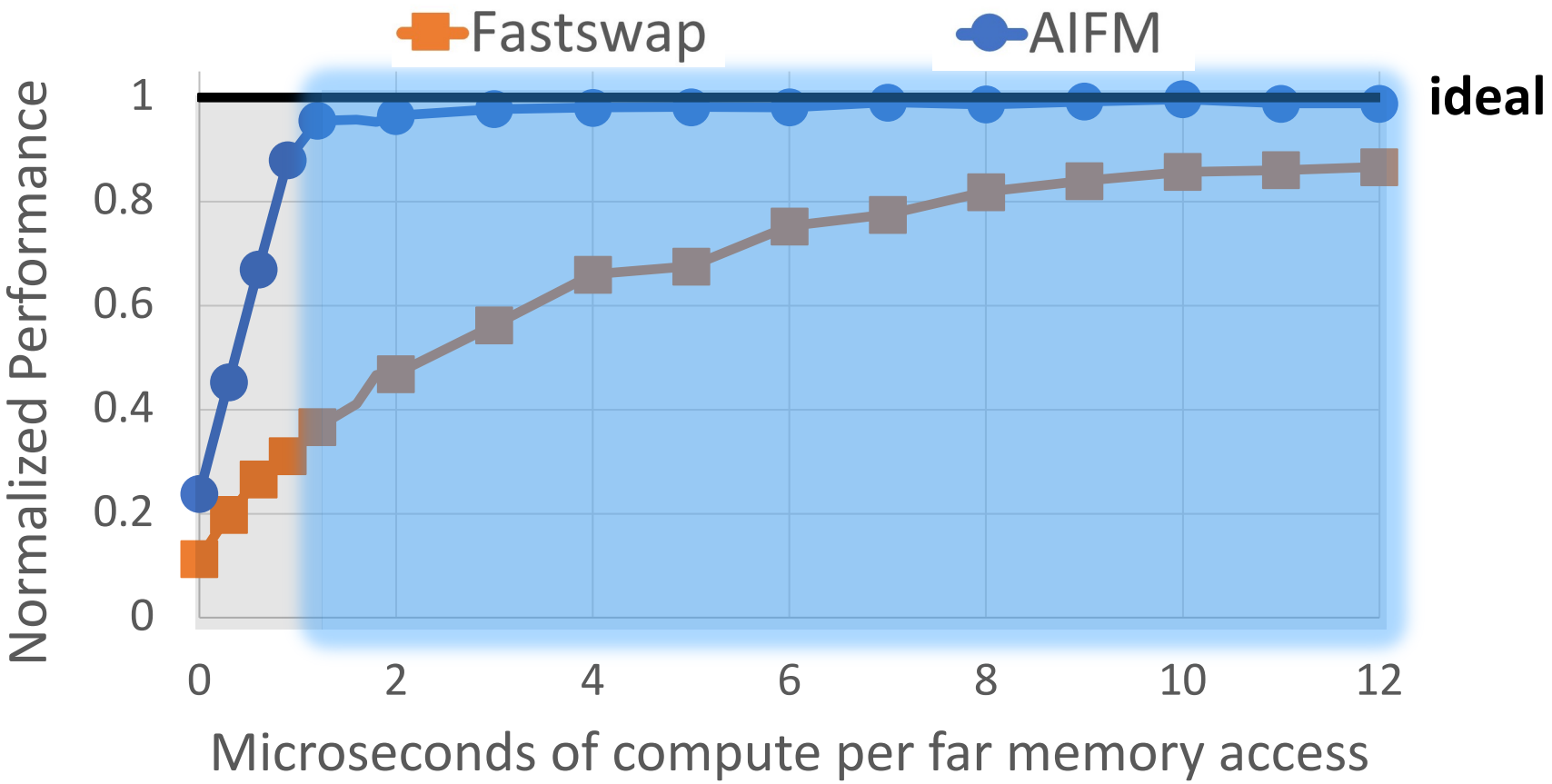

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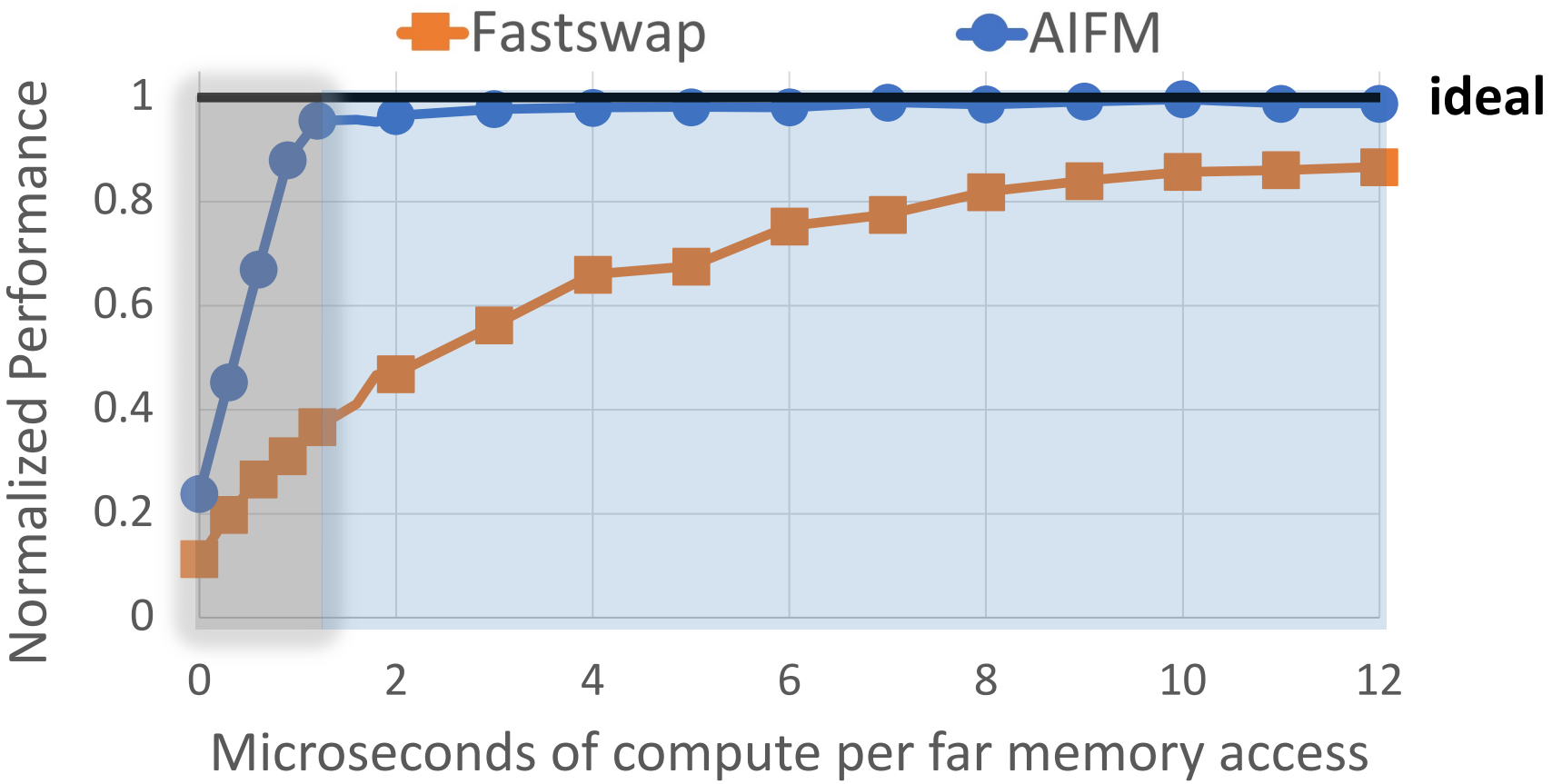

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➢Keep complex operations locally and **offload** very light operations.

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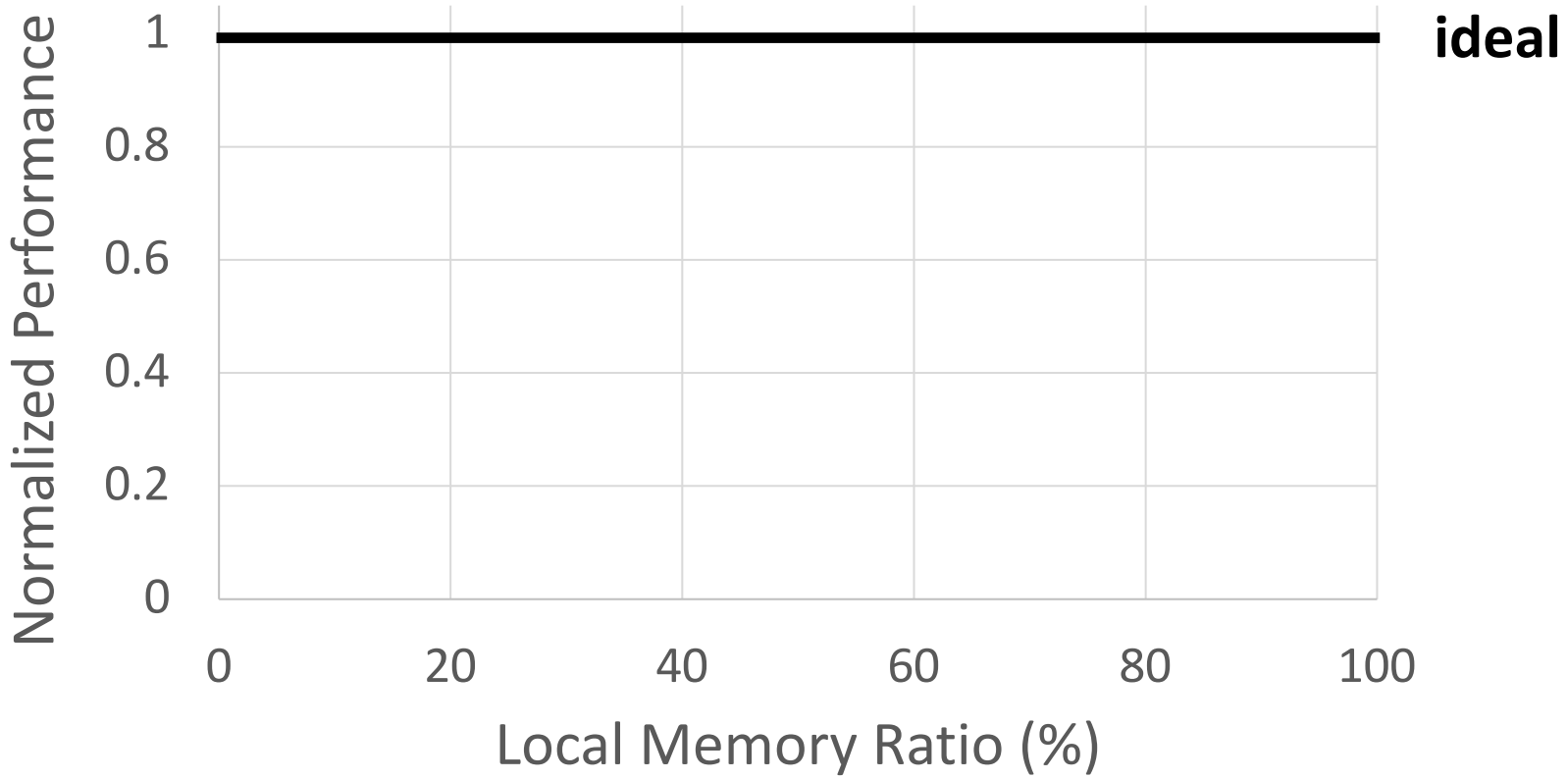

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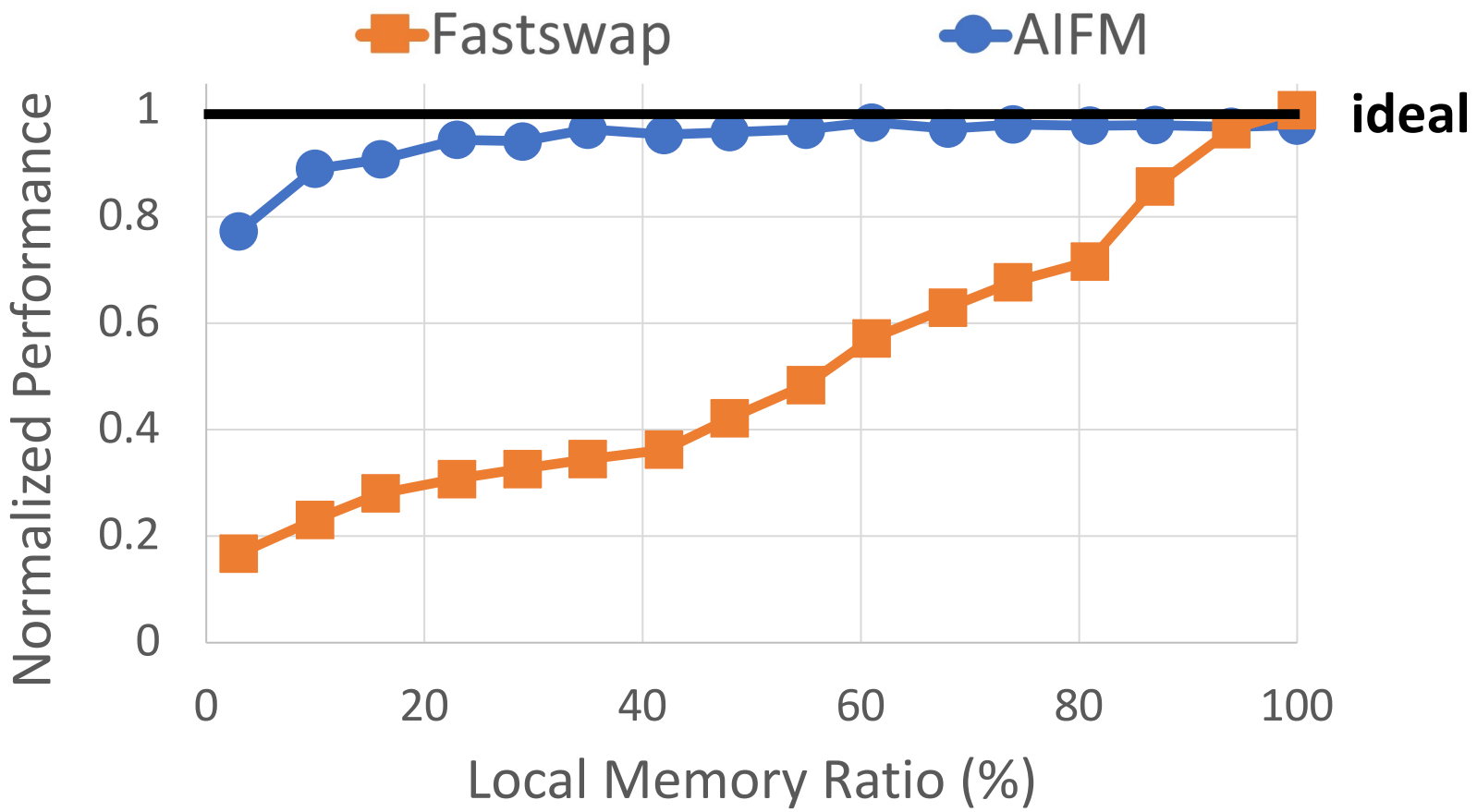

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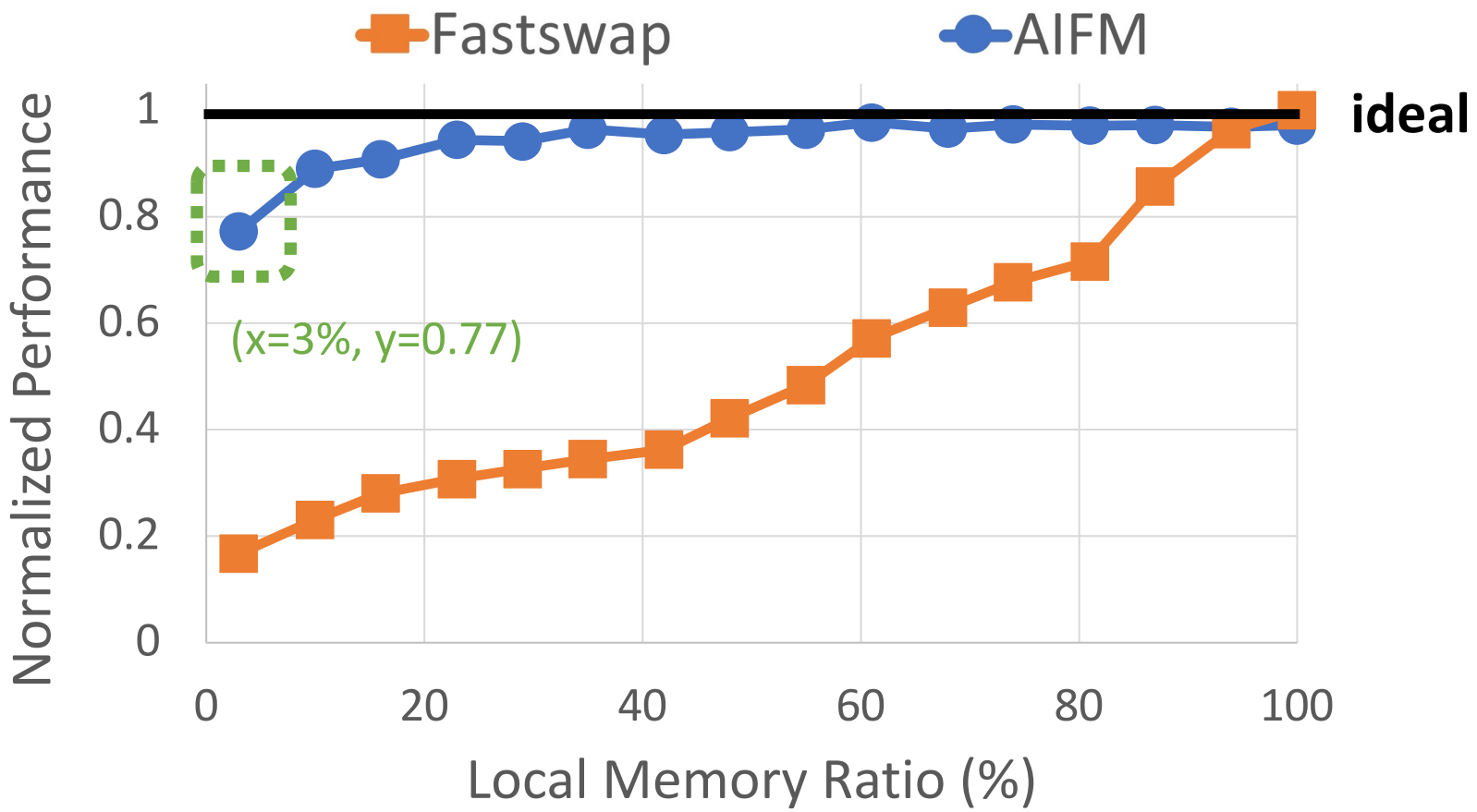

AIFM achieves near-ideal performance with small local memory.

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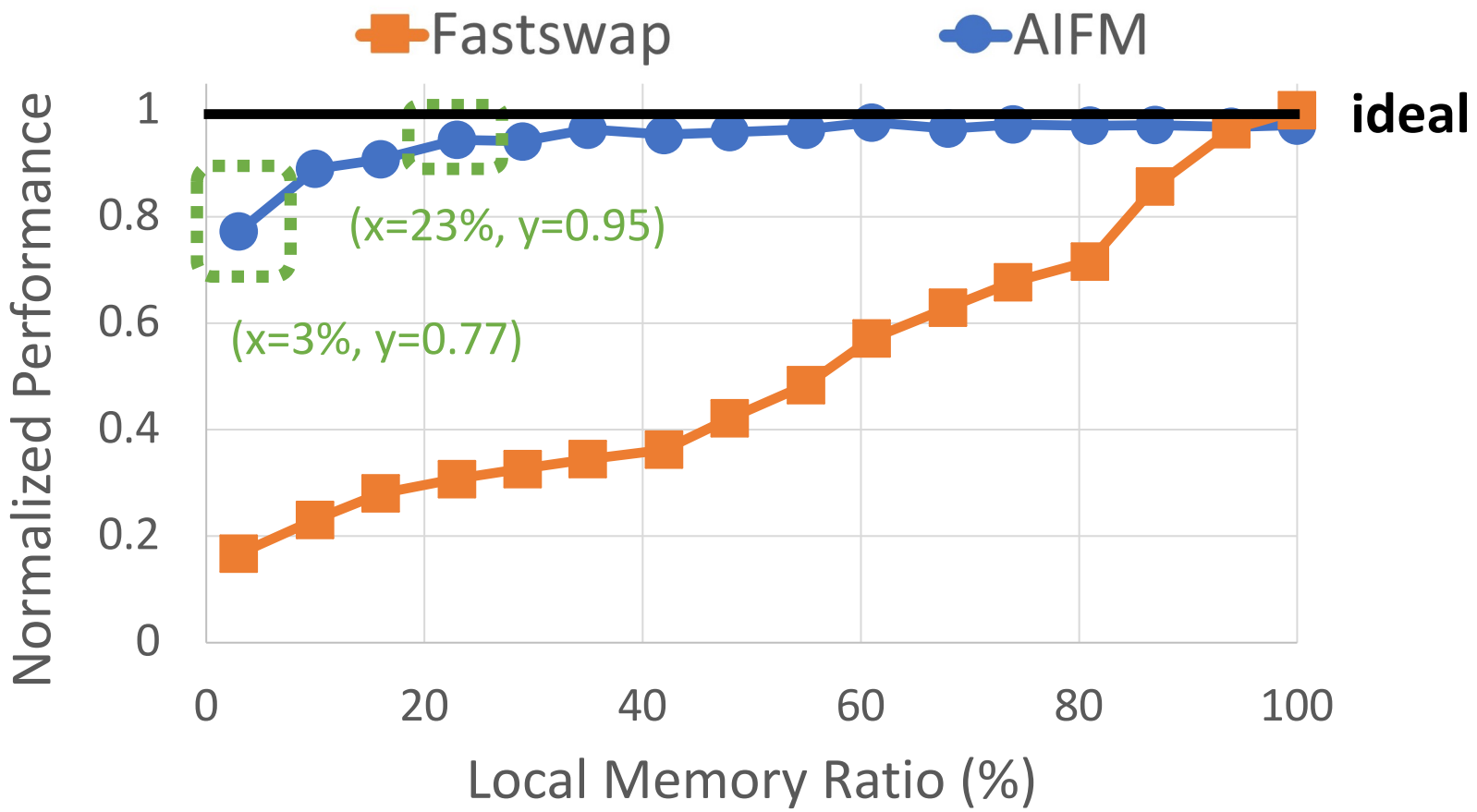

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➢Code released at https://github.com/AIFM-sys/AIFM